Statistical Performance Modeling and Optimization

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Abstract

As IC technologies scale to finer feature sizes, it becomes increasingly difficult to control the relative process variations. The increasing fluctuations in manufacturing processes have introduced unavoidable and significant uncertainty in circuit performance; hence ensuring manufacturability has been identified as one of the top priorities of today's IC design problems. In this paper, we review various statistical methodologies that have been recently developed to model, analyze, and optimize performance variations at both transistor level and system level. The following topics will be discussed in detail: sources of process variations, variation characterization and modeling, Monte Carlo analysis, response surface modeling, statistical timing and leakage analysis, probability distribution extraction, parametric yield estimation and robust IC optimization. These techniques provide the necessary CAD infrastructure that facilitates the bold move from deterministic, corner-based IC design toward statistical and probabilistic design.

Contents

1

Introduction

As integrated circuit (IC) technologies continue shrinking to nanoscale, there is increasing uncertainty in manufacturing process which makes it continually more challenging to create a reliable, robust design that will work properly under all manufacturing fluctuations. Large-scale process variations have already become critical and can significantly impact circuit performance even for today's technologies [14, 72, 73, 100]. Figure 1.1 shows the relative process variations (3σ/mean) predicted by the International Technology Roadmap for Semiconductors (ITRS) [100]. These large-scale variations introduce numerous uncertainties in circuit behavior and make it more difficult than ever to achieve a robust IC design.

In addition, when we consider some of the promising new device structures (e.g., carbon nano-tube [8, 34], FinFET [20], etc.) that have been recently proposed to maintain the aggressive pace of IC technology scaling, it is apparent that applying them to high-volume production will be a challenging problem due to the manufacturing uncertainty, or even their likelihood of failure. While it has already become extremely difficult to reliably manufacture nano-scale devices and achieve high product *yield* (defined as the proportion of the manufactured chips

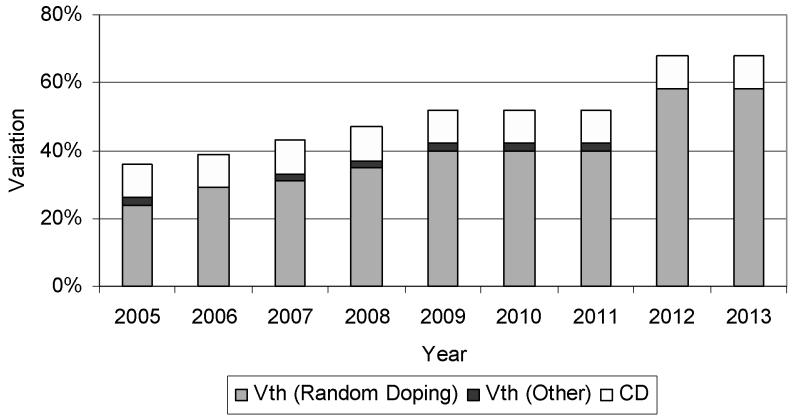

Fig. 1.1 Relative process variations (3σ/mean) predicted by [100].

that function correctly) with today's technologies, it would be almost impossible to do so affordably with tomorrow's technologies using existing deterministic design methodologies. For this reason, a paradigm shift in IC design is required to simultaneously improve circuit performance and product yield when using manufacturing technologies that present significant uncertainty.

The yield loss in a manufacturing process can be classified into two broad categories: *catastrophic* (due to physical and structural defects, e.g., open, short, etc.) and *parametric* (due to parametric variations in process parameters, e.g., V_{TH}, T_{OX}, etc.). As process variations become relatively large due to technology scaling, parametric yield loss is becoming increasingly significant at 90 nm technologies and beyond. Therefore, we focus on the parametric yield problem in this paper. We will review a number of recently-developed techniques that handle large-scale process variations at both transistor and system levels to facilitate affordable statistical integrated circuit design. Especially, we will focus on the following two questions:

- *When should process variations be considered?* Ideally, we want to take into account process variations in the earliest design stage. However, this strategy may not be necessary and/or efficient in practice. During early-stage system-level

design, many simplified models must be used to make the large-scale design problem tractable. The errors of these system-level models may be comparable to, or even larger than, the uncertainties caused by process variations. In such cases, it is not meaningful to model and analyze process variations at system level. As the design moves from system level down to circuit level, more accurate circuit-level models become available. We should start to consider process variations at the stage where circuit models are sufficiently accurate and process variations become the dominant uncertainties that impact performance.

- *How should process variations be considered?* For example, the simplest way to model process variations is to define a number of process corners. That is, every process parameter is assigned with a lower bound and an upper bound, and the best-case and worst-case circuit performances are computed by enumerating all possible combinations of the extreme values of process parameters. The aforementioned corner model is simple; however, such a corner-based approach may result in large error, since it completely ignores the correlation among different process parameters. In addition, it is not guaranteed that the best/worst-case performance always occurs at one of these corners. An alternative approach to model process variations is to use statistical device models where process parameters are modeled as random variables. (More details on statistical device models can be found in Chapter 2.) The statistical device model is much more accurate, but also expensive, than the traditional corner model.

One of the major objectives of this paper is to review and compare different statistical IC analysis and optimization techniques, and analyze their trade-offs for practical industrial applications. The following topics will be covered in this paper:

- *Sources of process variations and their models.* We will briefly review both front-end of line (FEOL) variations and back-end of line (BEOL) variations in Chapter 2. Several

techniques for variation characterization and modeling will be presented for both device-level and chip-level applications.

- *Transistor-level statistical methodologies.* In Chapter 3, we will discuss and compare a number of transistor-level statistical modeling, analysis and optimization techniques. In particular, the following topics will be covered: Monte Carlo analysis, response surface modeling, probability distribution extraction, parametric yield estimation, and robust transistor-level optimization. Several recently-developed methodologies, including projection-based performance modeling (PROBE) and asymptotic probability extraction (APEX), will be described in detail.
- *System-level statistical methodologies.* Most system-level statistical analysis and optimization techniques utilize a hierarchical flow to partition the entire system into multiple small blocks such that the large-size problem becomes tractable. In Chapter 4, we will discuss a number of system-level statistical methodologies that have been recently proposed. In particular, we will focus on the statistical timing and leakage problems for large-scale digital systems.

Finally, we will conclude and propose several possible areas for future research in Chapter 5.

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