The Chip Is the Network: Toward a Science of Network-on-Chip Design

The Chip Is the Network: Toward a Science of Network-on-Chip Design

Radu Marculescu

Carnegie Mellon University
Pittsburgh, PA 15213
USA
radum@ece.cmu.edu

Paul Bogdan

Carnegie Mellon University
Pittsburgh, PA 15213
USA
pbogdan@ece.cmu.edu

now
the essence of knowledge

Boston – Delft

Foundations and Trends® in Electronic Design Automation

Published, sold and distributed by:
now Publishers Inc.
PO Box 1024
Hanover, MA 02339
USA
Tel. +1-781-985-4510
www.nowpublishers.com
sales@nowpublishers.com

Outside North America:
now Publishers Inc.
PO Box 179
2600 AD Delft
The Netherlands
Tel. +31-6-51115274

The preferred citation for this publication is R. Marculescu and P. Bogdan, The Chip Is the Network: Toward a Science of Network-on-Chip Design, Foundations and Trends® in Electronic Design Automation, vol 2, no 4, pp 371–461, 2007

ISBN: 978-1-60198-192-9

Foundations and Trends® in
Electronic Design Automation
Volume 2 Issue 4, 2007

Editorial Scope

Foundations and Trends® in Electronic Design Automation will publish survey and tutorial articles in the following topics:

- System Level Design
- Behavioral Synthesis
- Logic Design
- Verification
- Test
- Physical Design
- Circuit Level Design
- Reconfigurable Systems
- Analog Design

Information for Librarians

Foundations and Trends® in Electronic Design Automation, 2007, Volume 2, 4 issues. ISSN paper version 1551-3939. ISSN online version 1551-3947. Also available as a combined paper and online subscription.

Foundations and Trends® in
Electronic Design Automation
Vol. 2, No. 4 (2007) 371–461

DOI: 10.1561/1500000011

The Chip Is the Network: Toward a Science of Network-on-Chip Design

Radu Marculescu[1] and Paul Bogdan[2]

[1] *Department of Electrical and Computer Engineering, Carnegie Mellon University, 5000 Forbes Avenue, Pittsburgh, PA 15213, USA, radum@ece.cmu.edu*

[2] *Department of Electrical and Computer Engineering, Carnegie Mellon University, 5000 Forbes Avenue, Pittsburgh, PA 15213, USA, pbogdan@ece.cmu.edu*

Abstract

In this survey, we address the concept of network in three different contexts representing the deterministic, probabilistic, and statistical physics-inspired design paradigms. More precisely, we start by considering the natural representation of networks as graphs and discuss the main deterministic approaches to Network-on-Chip (NoC) design. Next, we introduce a probabilistic framework for network representation and optimization and present a few major approaches for NoC design proposed to date. Last but not least, we model the network as a thermodynamic system and discuss a statistical physics-based approach to characterize the network traffic. This formalism allows us to address the network concept in the most general context, point out the main limitations of the proposed solutions, and suggest a few open-ended problems.

Contents

1 Introduction **1**

2 Deterministic Perspective **7**

2.1 Representation 7
2.2 Problem Formulation 11
2.3 Literature Survey 19
2.4 Implementation Issues 36

3 Stochastic Perspective **43**

3.1 Representation 43
3.2 Problem Formulation 48
3.3 Literature Survey 56

4 Statistical Physics Perspective **65**

4.1 Representation 65
4.2 Literature Survey 66

Acknowledgments **75**

References **77**

1

Introduction

Living in a world where the concept of *network* is ubiquitous, makes the quest for a science of network design inevitable. Informally speaking, the science of network design seeks to discover and explain the main properties affecting the network structure and behavior, as well as the mathematical models for predicting their dynamics and guiding their implementation.

The science of networks is primarily based on the graph theory, one of the most successful developments in mathematics ever. Indeed, the graph theory has led to an incredible number of real life applications that continue to grow even today. The graph theory originates in 1736 when Leonhard Euler offered the first rigorous solution to the "Seven Bridges of Konigsberg" problem. More precisely, by abstracting each landmass with a node (or vertex) and each bridge with an edge (link) (see Figure 1.1), Euler was able to show that a path that crosses all seven bridges in the city of Konigsberg only once cannot exist [18]. The newly proposed modeling paradigm based on sets of points linked by edges and represented via adjacency matrices (i.e., a matrix of zeros and ones, where each row in the matrix represents the connectivity of a node) has found many real-world applications. For instance, Cayley

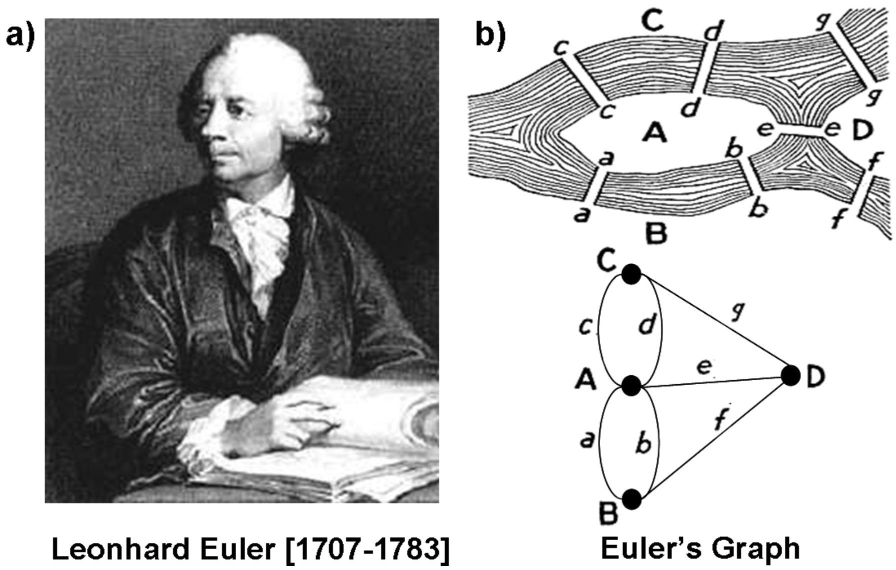

Fig. 1.1 Deterministic perspective on networks: (a) Leonhard Euler invented graph theory while trying to show that a path crossing all bridges in Konigsberg does not exist. (b) Abstract representation of the "Seven Bridges of Konigsberg" problem: river sides are depicted as nodes and bridges as arcs.

graphs have been applied in the field of chemistry for studying various compound molecules [14]. Other applications of static graphs include the graph coloring with applications to register allocation, scheduling and compiler design; construction of trees with applications in designing the railway system; the problem of finding the optimal cycle in a graph (i.e., the traveling salesman problem) with application to VLSI design; computation of voltages and currents in electric circuits via Kirchhoff's law [38].

Almost two centuries after the "Seven Bridges of Konigsberg" problem was solved, a new discovery in the graph theory, namely the *random graphs* proposed by Erdos and Renyi [68, 69], revolutionized the way we perceive real systems (e.g., rail, road, airplane, electronic networks, etc.). Random graphs are similar to regular graphs with the distinction that any edge between two arbitrary nodes is established with a certain probability. Consequently, the corresponding entry in the adjacency matrix is the probability $p \in [0,1]$ that two nodes are connected (instead of a fixed 1 value which would correspond to the classical graph model). This way, a new bridge is created between graph and probability theories [35]; this introduces the possibility of naturally modeling social communication, collaboration or biological networks [62, 140].

Understanding the network behavior requires a deep analysis of the topology and pattern of communication among network components. Thus, a breakthrough in the field of graph theory took place in the 1990s, when physicists questioned the evolution and structure of real networks [8, 71, 78]. The fundamental contribution of this new body of work is the replacement of the static view of random graphs with a dynamic view based on probability distributions for node connectivity in the hope of finding the optimal design of any communication network.

In recent years, the level of understanding of networking concepts needed to design and control complex systems, has reached unprecedented peaks. As such, a holistic approach to the network paradigm is essential. Such an approach involves understanding the theoretical basis (e.g., graph theory, stochastic modeling and analysis), the essential properties (e.g., structure, dynamics, communication paradigm), and the metrics (e.g., energy, fault-tolerance, robustness) which are relevant to designing and characterizing different networks in either engineered or biological systems.

In order to put the network concept into the proper perspective, we need to step back and consider Milner's fundamental work on calculus of communicating systems (also referred to as process algebra) [132], which enables the compact description of communication actions between any two agents. Inspired by the synergy between concurrency and communication, the design of electronic systems has moved recently from computation-based design to communication-based design. Indeed, nowadays, Systems-on-Chips (SoCs) represent true distributed systems at nanoscale where communication aspects dominate. From a technology point of view, this paradigm shift is intended to mitigate the problem of interconnects, keep the design complexity under control, and reduce costs. Since none of the classical architectures based on point-to-point or bus-based communication scales nicely in terms of power and performance figures, a networked architecture based on packet switching has been suggested for future multicore systems [58].

Starting from these overarching ideas, in this survey we address the concept of network in Multiprocessor Systems-on-Chip (MPSoCs) and identify specific design principles and optimization techniques that are relevant to the design automation research community. Understanding the structure and behavior of seemingly different networks is crucial for our ability to master complex behaviors that characterize the emergent application domains. For instance, for SoCs, it has been suggested to replace the global interconnects with packet switching communication via the Network-on-Chip (NoC) paradigm [22, 30, 87, 88, 102] and then avoid the interconnect performance issues [91, 115], while allowing for higher level of fault-tolerance in Deep Submicron (DSM) technologies [24, 167]. Several concrete NoC architectures have been investigated in the literature [61, 116, 198, 201], as well as energy-efficient Globally Asynchronous Locally Synchronous (GALS) designs [20, 21, 42, 181, 212].

The emergent NoC communication paradigm consists of exchanging packets of information among various nodes in the network. As shown in Figure 1.2, each node consists of a core (e.g., DSP or CPU modules, video processors, embedded memory blocks or application specific Processing Elements (PEs)) and a router meant to forward the incoming packets toward the appropriate destination according to the header information. To support the inter-tile communication, each core has embedded input and output buffers to temporarily store the incoming packets from the neighboring nodes in the network. For instance, a packet generated at source (1,1) that needs to be delivered to destination (2,3) via a static XY routing, is first sent from the local PE to its associated router at tile (1,1); then, at each intermediate node, a routing decision is made based on the header information as shown with the dotted arrows in Figure 1.2 for the shortest source–destination path. To avoid the stalling of information flow due to the dependencies on network resources (i.e., shared routing paths), the concept of virtual channels (VCs) has been introduced as well [57, 114, 133, 141]. VCs share dedicated links and provide multiple buffers for each channel.

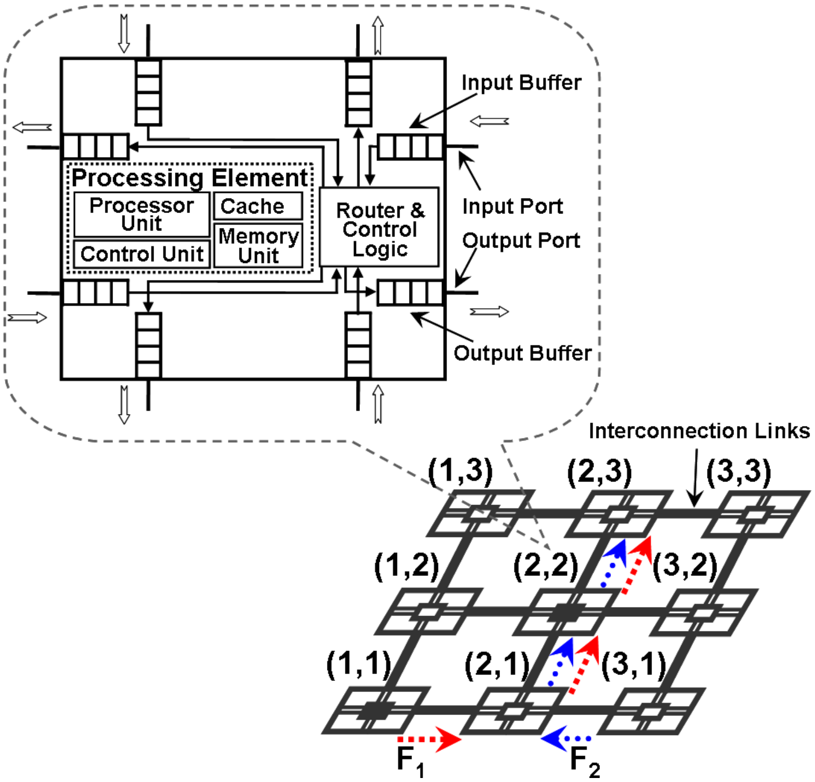

Fig. 1.2 A 3×3 mesh Network-on-Chip (NoC) architecture consisting of Processing Elements (PEs), routers, and interconnection links. Flows F_1 and F_2 are used to depict a stalling problem along the path from node (2,1) to (2,3) which can be solved by utilizing virtual channels.

For instance, the problem of stalling the flow F_1 from (1,1) to (2,3) due to a flow F_2 from (3,1) to (2,3), is solved by reserving the VCs between nodes (2,1), (2,2), and (2,3) for F_1.

A natural question now is what are the fundamental mathematical techniques that can be used to design, control, and optimize such networks in a rigorous manner. One such powerful technique is the *linear programming* (LP) approach used to solve maximum flow problems [54]. The goal of the linear program is to find a legal flow assignment of the edges of a given graph satisfying the flow conservation constraints. Another mathematical programming approach, namely the *quadratic programming* (QP) was proposed for solving the max-cut problem [54, 86]. Due to the requirement of discrete values, many real world optimization problems need an integer analysis done either via integer or mixed integer linear programming [156]. For small problems, efficient algorithms such as branch-and-bound or LP-relaxation have been proposed. However, for large problems, the solution is still based on heuristics.

Early studies of the network dynamics use queueing theory first developed by Markov [128] and Erlang [70], formalized by Kolmogorov [112] and Kendall [104], and extensively used in the context of packet switching networks by Kleinrock [110]. Nonetheless, in order to ease the mathematical tractability, most queueing approaches rely on exponential type distributions for the event/job arrival and/or service time. As shown in several studies, this may not be an accurate model for the real network traffic. Consequently, one of our objectives in this survey is to also highlight alternatives to the conventional paradigm of network design. This new vision is based on rigorous developments in the field of statistical physics and information theory that allow us to model the network as a thermodynamical system. The hope is that this new modeling paradigm enables not only capturing the intrinsic interactions among various network components, but also helps proposing more powerful techniques for predicting and optimizing the network.

These ideas are detailed in the remainder of this survey. More precisely, Section 2 presents a graph-based formalism for the network design and the major approaches proposed in a deterministic setup. Section 3 takes a probabilistic view on designing NoC architectures under the Markovian assumption. Finally, Section 4 introduces new problems in a statistical physics-based context for network design and enumerates some preliminary steps taken toward solving these problems.

References

[1] P. Abad, V. Puente, J. A. Gregorio, and P. Prieto, "Rotary router: An efficient architecture for CMP interconnection networks," *ACM SIGARCH Computer Architecture News*, vol. 35, no. 2, May 2007.

[2] A. Adriahantenaina and A. Greiner, "Micro-network for SoC: Implementation of a 32-Port SPIN network," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, March 2003.

[3] V. S. Adve and M. K. Vernon, "Performance analysis of mesh interconnection networks with deterministic routing," *IEEE Transactions on Parallel and Distributed Systems*, vol. 5, no. 3, pp. 225–246, March 1994.

[4] S. N. Adya and I. L. Markov, "Fixed-outline floorplanning: Enabling hierarchical design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 6, pp. 1120–1135, December 2003.

[5] A. Agarwal, "Limits on Interconnection Network Performance," *Transactions on Parallel and Distributed Systems*, vol. 2, no. 4, October 1991.

[6] J. Ahn and S. Kang, "Test scheduling of NoC-based SoCs using multiple test clocks," *Electronics and Telecommunications Research Institute Journal*, vol. 28, no. 4, pp. 475–485, August 2006.

[7] R. Ahuha, T. Magnanti, and J. Orlin, *Network Flows: Theory, Algorithms, and Applications.* Prentice Hall, 1993.

[8] R. Albert and A.-L. Barabasi, "Statistical mechanics of complex networks," *Reviews of Modern Physics*, vol. 47, p. 74, cond-mat/0106096, 2002.

[9] A. M. Amory, E. Briao, E. Cota, M. Lubaszewski, and F. G. Moraes, "A scalable test strategy for network-on-chip routers," in *Proceedings of IEEE International Test Conference*, November 2005.

[10] F. Angiolini, D. Atienza, S. Murali, L. Benini, and G. De Micheli, "Reliability support for on-chip memories using networks-on-chip," in *Proceedings of the International Conference on Computer Design (ICCD)*, October 2006.

[11] F. Angiolini, P. Meloni, S. Carta, L. Benini, and L. Raffo, "Contrasting a NoC and a traditional interconnect fabric with layout awareness," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, March 2006.

[12] Arteris [online]. Available: http://www.arteris.com.

[13] G. Ascia, V. Catania, and M. Palesi, "Multi-objective mapping for mesh-based NoC architectures," in *Proceedings of the 2nd IEEE/ACM/IFIP International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)*, pp. 182–187, September 2004.

[14] A. T. Balaban, *Chemical Applications of Graph Theory*. Academic Press, 1976.

[15] J. Balfour and W. J. Dally, "Design tradeoffs for tiled CMP on-chip networks," in *Proceedings of the 20th International Conference on Supercomputing (ICS)*, pp. 187–198, June 2006.

[16] M. Ball, C. Cifuentes, and B. Deepankar, "Partitioning of code for a massively parallel machine," in *Proceedings of the 13th International Conference on Parallel Architecture and Compilation Techniques (PACT)*, pp. 225–236, September 2004.

[17] N. Banerjee, P. Vellank, and K. S. Chatha, "A power and performance model for network-on-chip architectures," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, p. 21250, February 2004.

[18] A.-L. Barabási, *Linked: How Everything is Connected to Everything Else*. Plume Books, 2004.

[19] T. A. Bartic, J. y. Mignolet, V. Nollet, T. Marescaux, D. Verkest, S. Vernalde, and R. Lauwereins, "Highly scalable network on chip for reconfigurable systems," in *Proceedings of the International Symposium on System-on-Chip*, pp. 79–82, November 2003.

[20] P. Beerel and M. E. Roncken, "Low power and energy efficient asynchronous design," *Journal of Low Power Electronics*, vol. 3, no. 3, pp. 234–253, December 2007.

[21] E. Beigne, F. Clermidy, S. Miermont, and P. Vivet, "Dynamic voltage and frequency scaling architecture for units integration with a GALS NoC," in *Proceedings of the 2nd ACM/IEEE International Symposium on Network-on-Chip (NOCS)*, pp. 129–138, 2008.

[22] L. Benini and G. De Micheli, "Networks on chips: A new SoC paradigm," *IEEE Computer*, vol. 35, no. 1, January 2002.

[23] D. Berstsekas and R. Gallager, *Data Networks*. Prentice Hall, 1992.

[24] D. Bertozzi, L. Benini, and G. De Micheli, "Error control schemes for on-chip communication links: The energy-reliability tradeoff," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 6, pp. 818–831, June 2005.

[25] D. Bertozzi, A. Jalabert, S. Murali, R. Tamhankar, S. Stergiou, L. Benini, and G. De Micheli, "NoC synthesis flow for customized domain specific multiprocessor systems-on-chip," *IEEE Transactions on Parallel and Distributed Systems*, vol. 16, no. 2, pp. 113–129, February 2005.

[26] S. Bertozzi, A. Acquaviva, D. Bertozzi, and A. Poggiali, "Supporting task migration in multi-processor systems-on-chip: A feasibility study," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, March 2006.

[27] P. S. Bhojwani and R. N. Mahapatra, "Interfacing cores with on-chip packet-switched networks," in *Proceedings of the International Conference on VLSI Design*, 2003.

[28] P. S. Bhojwani and R. N. Mahapatra, "A robust protocol for concurrent on-Line test (COLT) of noc-based systems-on-a-chip," in *Proceedings of Design Automation Conference*, June 2007.

[29] G. Bianconi and A.-L. Barabási, "Bose-Einstein condensation in complex networks," *Physical Review Letters*, vol. 86, pp. 5632–5635, 2001.

[30] T. Bjerregaard and S. Mahadevan, "A survey of research and practices of network-on-chip," *ACM Computing Surveys*, vol. 38, no. 1, March 2006.

[31] P. Bogdan, T. Dumitras, and R. Marculescu, "Stochastic communication: A new paradigm for fault-tolerant networks-on-chip," *Hindawi VLSI Design*, February 2007.

[32] P. Bogdan and R. Marculescu, "Quantum-like effects in network-on-chip buffers behavior," in *Proceedings of the 44th Design Automation Conference (DAC)*, pp. 266–267, ACM, NY, 2007.

[33] P. Bogdan and R. Marculescu, "Hitting time analysis for stochastic communication," in *Proceedings of the International Conference on Nano-Networks*, Boston, September 2008.

[34] G. Bolch, S. Greiner, H. de Meer, and K. S. Trivedi, *Queueing Networks and Markov Chains: Modeling and Performance evaluation with Computer Science Applications*. John Wiley and Sons, 2006.

[35] B. Bollobas, *Random Graphs*. Cambridge University Press, second ed., 2001.

[36] E. Bolotin, I. Cidon, R. Ginosar, and A. Kolodny, "QNoC: QoS architecture and design process for network on chip," *Journal of Systems Architecture (EUROMICRO)*, vol. 50, nos. 2–3, pp. 105–128, February 2004.

[37] E. Bolotin, I. Cidon, R. Ginosar, and A. Kolodny, "Routing table minimization for irregular mesh NoCs," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, April 2007.

[38] A. J. Bondy and U. S. R. Murty, *Graph Theory with Applications*. John Wiley and Sons, 2005.

[39] D. Borrione, "A generic model for formally verifying NoC communication architectures: A case study," in *Proceedings of the First International Symposium Networks-on-Chip (NOCS)*, pp. 127–136, 2007.

[40] S. Brandt and H. D. Dahmen, *The Picture Book of Quantum Mechanics*. Springer, 2001.

[41] M. J. Brusco and S. Stahl, *Branch-and-Bound Applications in Combinatorial Data Analysis*. New York, NY: Springer, 2005.

[42] G. Campobello, M. Castano, C. Ciofi, and D. Mangano, "GALS networks on chip: A new solution for asynchronous delay-insensitive links," in *Proceedings of Design, Automation and Test in Europe Conference (DATE)*, March 2006.

[43] L. P. Carloni, K. L. McMillan, and A. L. Sangiovanni-Vincentelli, "Theory of latency-insensitive design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 9, pp. 1059–1076, September 2001.
[44] J. M. Carlson and J. Doyle, "Highly optimized tolerance: Robustness and design in complex systems," *Physical Review Letter*, vol. 84, no. 11, 2000.
[45] V. Catania, R. Holsmark, S. Kumar, and M. Palesi, "A methodology for design of application specific deadlock-free routing algorithms for NoC systems," in *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, October 2006.
[46] J. Chan and S. Parameswaran, "NoCEE: Energy macro-model extraction methodology for network on chip routers," in *Proceedings the of International Conference on Computer Aided Design (ICCAD)*, November 2005.
[47] M. F. Chang, J. Cong, A. Kaplan, M. Naik, G. Reinman, E. Socher, and S. W. Tam, "CMP network-on-chip overlaid with multi-band RFinterconnect," in *Proceedings of the International Symposium on High-Performance Computer Architecture (HPCA)*, February 2008.
[48] X. Chen and L.-S. Peh, "Leakage power modeling and optimization in interconnection networks," in *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, August 2003.
[49] C.-L. Chou, U. Y. Ogras, and R. Marculescu, "Energy- and performance-aware incremental mapping for networks-on-chip with multiple voltage levels," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 10, October 2008.
[50] I. Cohen, O. Rottenstreich, and I. Keslassy, "Statistical approach to NoC design," in *Proceedings of the Second ACM/IEEE International Symposium Networks-on-Chip (NOCS)*, Newcastle, UK, April 2008.
[51] M. Colajanni, B. Ciciani, and F. Quaglia, "Performance analysis of wormhole switching with adaptive routing in a two-dimensional torus," in *Proceedings of the 5th International Euro-Par Conference on Parallel Processing, Lecture Notes in Computer Science*, 1999.
[52] Communication Synthesis Infrastructure [Online]. Available: http:// embedded.eecs.berkeley.edu/cosi/.
[53] C. Constantinescu, "Impact of deep submicron technology on dependability of VLSI circuits," in *Proceedings of the 2002 International Conference on Dependable Systems and Networks (DSN)*, pp. 205–209, June 23–26 2002.
[54] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein, *Introduction to Algorithms.* MIT Press and McGraw-Hill, Second ed., 2001.
[55] A. K. Coskun, T. S. Rosing, and K. Whisnant, "Temperature aware task scheduling in MPSoCs," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, April 2007.
[56] W. J. Dally, "Performance analysis of k-ary n-cube interconnection networks," *IEEE Transactions on Computers*, vol. 39, no. 6, June 1990.
[57] W. J. Dally, "Virtual-channel flow control," *IEEE Transactions on Parallel and Distributed Systems*, vol. 3, no. 2, pp. 194–205, March 1992.

[58] W. J. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks," in *Proceedings of the Design Automation Conference (DAC)*, June 2001.

[59] W. J. Dally and B. Towles, *Principles and Practices of Interconnection Networks*. Morgan Kaufmann, 2004.

[60] G. De Micheli and L. Benini, *Networks on Chips: Technology and Tools*. Morgan Kaufmann, 2006.

[61] J. Dielissen, A. Radulescu, K. Goossens, and E. Rijpkema, "Concepts and implementation of the Philips network-on-chip," in *Proceedings of the IP-based SoC Design*, November 2003.

[62] S. N. Dorogovtsev and J. F. F. Mendes, *Evolution of Networks: From Biological Networks to the Internet and WWW*. Oxford University Press, 2003.

[63] J. Draper and J. Ghosh, "A comprehensive analytical model for wormhole routing in multicomputer systems," *Journal of Parallel and Distributed Computing*, vol. 23, no. 2, November 1994.

[64] J. Duato, S. Yalamanchili, and L. Ni, *Interconnection Networks: An Engineering Approach*. San Mateo, CA: Morgan Kaufmann, 2002.

[65] T. Dumitras, S. Kerner, and R. Marculescu, "Towards on-chip fault-tolerant communication," in *Proceedings of the 2003 Conference on Asia South Pacific Design Automation (ASP-DAC)*, Kitakyushu, Japan, January 21–24 2003.

[66] N. Eisley and L.-S. Peh, "High-level power analysis for on-chip networks," in *Proceedings of the 2004 International Conference on Compilers, Architecture, and Synthesis For Embedded Systems (CAES)*, Washington DC, USA, September 22–25 2004.

[67] A. Ejlali, B. M. Al-Hashimi, P. Rosinger, and S. G. Miremadi, "Joint consideration of fault-tolerance, energy-efficiency and performance in on-chip networks," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, April 2007.

[68] P. Erdos and A. Renyi, "On random graphs," *Publicationes Mathematicae Debrecen*, vol. 6, p. 290, 1959.

[69] P. Erdos and A. Renyi, "On the evolution of random grpahs," *Publicationes Mathematicae Institut Hungary Academic Science*, vol. 5, p. 17, 1960.

[70] A. K. Erlang, "The theory of probabilities and telephone conversations," *Nyt Tidsskrift for Matematik B*, vol. 20, 1909.

[71] M. Faloutsos, P. Faloutsos, and C. Faloutsos, "On power-law relationships of the internet topology," *Computer Communication Review*, vol. 29, p. 251, 1999.

[72] M. A. Faruque and J. Henkel, "Minimizing virtual channel buffer for routers in on-chip communication architectures," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, 2008.

[73] C. M. Fiduccia and R. M. Mattheyses, "A linear-time heuristic for improving network partitions," in *Proceedings of the Design Automation Conference (DAC)*, 1982.

[74] M. Franceschetti, M. D. Migliore, and P. Minero, "The capacity of wireless networks: Information-theoretic and physical limits," *IEEE Transaction on Information Theory*, 2007.

[75] H. Fuks and A. Lawniczak, "Performance of data networks with random links," *Mathematics and Computers in Simulation*, vol. 51, pp. 101–117, December 1999.

[76] A. Ghosh and S. Boyd, "Growing well-connected graphs," in *Proceedings of IEEE Conference on Decision and Control*, December 2006.

[77] K. Goossens, J. Dielissen, O. P. Gangwal, S. G. Pestana, A. Radulescu, and E. Rijpkema, "A design flow for application-specific networks-on-chip with guaranteed performance to accelerate SoC design and verification," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, March 2005.

[78] R. Govindan and H. Tangmunarunkit, "Heuristics for internet map discovery," *IEEE — INFOCOM*, 2000.

[79] P. Gratz, C. Kim, R. McDonald, S. W. Keckler, and D. C. Burger, "Implementation and evaluation of on-chip network architectures," in *Proceedings of the International Conference on Computer Design (ICCD)*, October 2006.

[80] C. Grecu, P. P. Pande, B. Wang, A. Ivanov, and R. Saleh, "Methodologies and algorithms for testing switch-based NoC interconnects," in *Proceedings of the 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, October 03–05 2005.

[81] F. Gruian, "Hard real-time scheduling for low energy using stochastic data and DVS processors," in *Proceedings of the International Symposium on Low-Power Electronics and Design*, August 2001.

[82] Q. P. Gu and S. Peng, "Wavelengths requirement for permutation routing in all-optical multistage interconnection networks," in *Proceedings of the 14th International Symposium on Parallel and Distributed Processing*, pp. 761–768, 2000.

[83] P. Guerrier and A. Greiner, "A generic architecture for on-chip packet switched interconnections," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, 2000.

[84] Z. Guz, I. Walter, E. Bolotin, I. Cidon, R. Ginosar, and A. Kolodny, "Efficient link capacity and QoS design for wormhole network-on-chip," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, March 2006.

[85] A. Hansson, K. Goossens, and A. Radulescu, "A unified approach to mapping and routing on a network-on-chip for both best-effort and guaranteed service traffic," *Hindawi VLSI Design*, May 2007.

[86] A. K. Hartmann and H. Rieger, *New Optimization Algorithms in Physics*. Wiley-VCH, 2004.

[87] A. Hemani, A. Jantsch, S. Kumar, A. Postula, and J. Oberg, "Network-on-chip: An architecture for billion transistor era," in *Proceedings of the IEEE NorChip Conference*, November 2000.

[88] J. Henkel, W. Wolf, and S. Chakradhar, "On-chip networks: A scalable communication-centric embedded system design paradigm," in *Proceedings of the 17th International Conference on VLSI Design*, pp. 845–851, January 2004.

[89] F. S. Hillier and G. J. Lieberman, *Introduction to Operations Research*. New York: McGraw-Hill, Ch.15, Sixth ed., pp. 661–732, 1995.

[90] W. H. Ho and T. M. Pinkston, "A methodology for designing efficient on-chip interconnects on well-behaved communication patterns," in *Proceedings of the International Symposium on High-Performance Computer Architecture*, February 2003.

[91] M. Horowitz, R. Ho, and K. Mai, "The future of wires," *Proceedings of IEEE*, vol. 89, no. 4, pp. 490–504, April 2001.

[92] J. Hu and R. Marculescu, "Energy-aware mapping for tile-based NOC architectures under performance constraints," in *Proceedings of the Conference on Asia South Pacific Design Automation (ASP-DAC)*, Kitakyushu, Japan, January 21–24 2003.

[93] J. Hu and R. Marculescu, "DyAD — Smart routing for networks-on-chip," in *Proceedings of the Design Automation Conference (DAC)*, June 2004.

[94] J. Hu and R. Marculescu, "Communication and task scheduling of application-specific networks-on-chip," *IEE Proceedings of Computers and Digital Techniques*, vol. 152, no. 5, pp. 643–651, September 2005.

[95] J. Hu and R. Marculescu, "Energy- and performance-aware mapping for regular NoC architectures," *IEEE Transactions on Computer-Aided Design Integrated Circuits and Systems*, vol. 24, no. 4, pp. 551–562, April 2005.

[96] J. Hu, U. Y. Ogras, and R. Marculescu, "System-level buffer allocation for application-specific networks-on-chip router design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 12, pp. 2919–2933, December 2006.

[97] P. Hu and L. Kleinrock, "An analytical model for wormhole routing with finite size input buffers," in *Proceedings of the 15th International Teletraffic Congress*, June 1997.

[98] T.-C. Huang, U. Y. Ogras, and R. Marculescu, "Virtual channels planning for networks-on-chip," in *Proceedings of the 8th International Symposium on Quality Electronic Design (ISQED)*, San Jose, March 2007.

[99] W. Hung, C. Addo-Quaye, T. Theocharides, Y. Xie, V. Narayanan, and M. J. Irwin, "Thermal-aware IP virtualization and placement for networks-on-chip architecture," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 11–13 2004.

[100] iNoCs Structured Interconnects [Online]. Available: http://www.inocs.com.

[101] A. Jalabert, S. Murali, L. Benini, and G. De Micheli, "xpipescompiler: A tool for instantiating application specific networks on chip," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, 2004.

[102] A. Jantsch and H. Tenhunen, *Networks-on-Chip*. Norwell, MA: Kluwer, 2003.

[103] Y. Jin, E. J. Kim, and K. H. Yum, "Peak power control for a QoS capable on-chip network," in *Proceedings of the International Conference on Parallel Processing (ICPP)*, June 14–17 2005.

[104] D. G. Kendall, "Some problems in the theory of queues," *Journal of Royal Statistical Society Series B*, vol. 13, pp. 230–264, 1951.

[105] D. Kim, K. Kim, J. Kim, S. Lee, and H. Yoo, "Solutions for real chip implementation issues of NoC and their application to memory-centric NoC," in *Proceedings of the First International Symposium on Networks-on-Chip (NOCS)*, pp. 30–39, May 2007.

[106] E. J. Kim, K. H. Yum, G. M. Link, C. R. Das, N. Vijaykrishnan, M. Kandemir, and M. J. Irwin, "Energy optimization techniques in cluster interconnects," in *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, Seoul, Korea, August 25–27 2003.

[107] J. Kim, W. J. Dally, and D. Abts, "Flattened butterfly: A cost-efficient topology for high-radix networks," in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

[108] M. Kim, D. Kim, and G. E. Sobelman, "Adaptive scheduling for CDMA based networks-on-chip," in *Proceedings of the IEEE Northeast Workshop on Circuits and Systems*, pp. 100–103, May 2005.

[109] S. Kirkpatrick, C. D. Gelatt, and M. P. Vecchi, "Optimization by simulated annealing," *Science*, vol. 220, no. 4598, pp. 671–680, 1983.

[110] L. Kleinrock, *Queueing Systems.* New York, NY: Wiley Interscience, 1976.

[111] T. Kogel, M. Doerper, A. Wieferink, R. Leupers, G. Ascheid, and H. Meyr, "A modular simulation framework for architectural exploration of on-chip interconnection networks," in *Proceedings of the 1st IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Newport Beach, CA, USA, October 01–03 2003.

[112] A. N. Kolmogorov, *Foundations of the Theory of Probability.* New York, NY: Chelsea Publishing Company, Second english ed., 1956.

[113] C. M. Krishna and K. G. Shin, *Real-time Systems.* McGraw-Hill, 1997.

[114] A. Kumar, L.-S. Peh, P. Kundu, and N. K. Jha, "Express virtual channels: Towards the ideal interconnection fabric," in *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007.

[115] R. Kumar, V. Zyuban, and D. M. Tullsen, "Interconnections in multi-core architectures: Understanding mechanisms, overheads and scaling," in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005.

[116] H. G. Lee, N. Chang, U. Y. Ogras, and R. Marculescu, "On-chip communication architecture exploration: A quantitative evaluation of point-to-point, bus and network-on-chip approaches," *ACM Transactions on Design Automation of Electronic Systems*, vol. 12, no. 3, August 2007.

[117] K. Lee, S. J. Lee, S. E. Kim, H. M. Choi, D. Kim, S. Kim, M. W. Lee, and H. J. Yoo, "A 51 mW 1.6 GHz on-chip network for low-power heterogeneous SoC platform," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 152–518, February 15–19 2004.

[118] T. Lehtonen, P. Liljeberg, and J. Plosila, "Fault tolerance analysis of NoC architectures," in *Proceedings of the International Symposium on Circuits and Systems (ISCAS)*, pp. 361–364, May 27–30 2007.

[119] T. Lei and S. Kumar, "A Two-step genetic algorithm for mapping task graphs to a network on chip architecture," in *Proceedings of the Euromicro Symposium on Digital System Design*, 2003.

[120] L. F. Leung and C. Y. Tsui, "Optimal link scheduling on improving best-effort and guaranteed services performance in network-on-chip system," in *Proceedings of the Design Automation Conference (DAC)*, July 2006.

[121] F. Li, G. Chen, and M. Kandemir, "Compiler-directed voltage scaling on communication links for reducing power consumption," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, 2005.

[122] J. Liang, A. Laffely, S. Srinivasan, and R. Tessier, "An architecture and compiler for scalable on-chip communication," *IEEE Transactions on Very-largescale Integration (VLSI) Systems*, vol. 12, no. 7, pp. 711–726, July 2004.

[123] J. Luo and N. K. Jha, "Power-conscious joint scheduling of periodic task graphs and aperiodic tasks in distributed real-time embedded systems," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, November 2000.

[124] B. B. Mandelbrot, *The Fractal Geometry of Nature*. San Francisco: Freeman Company, 1982.

[125] S. Manolache, P. Eles, and Z. Peng, "Fault and energy-aware communication mapping with guaranteed latency for applications implemented on NoC," in *Proceedings of the Design Automation Conference (DAC)*, July 2005.

[126] S. Manolache, P. Eles, and Z. Peng, "Buffer space optimisation with communication synthesis and traffic shaping for NoCs," in *Proceedings of the Design Automation and Test in Europe Conference*, Munich, Germany, March 6–10 2006.

[127] T. Marescaux and H. Corporaal, "Introducing the superGT network-on-chip," in *Proceedings of the Design Automation Conference (DAC)*, June 2007.

[128] A. A. Markov, "Extension of the law of large numbers to dependent events," *Bulletin Society Physics and Mathematics Kazan*, vol. 15, no. 2, no. 2, pp. 135–156, (in Russian), 1906.

[129] A. Messiah, *Quantum Mechanics: Two Volumes Bound as One*. Courier Dover Publications, 1999.

[130] S. Meyn and R. Tweedie, *Markov Chains and Stochastic Stability*. Springer Verlag, 2005.

[131] Z. Michalewicz and D. B. Fogel, *How to Solve it: Modern Heuristics*. Springer, 2000.

[132] R. Milner, *Communication and Concurrency*. Upper Saddle River, NJ, USA: Prentice-Hall, 1989.

[133] R. Mullins, A. West, and S. Moore, "Low-latency virtual-channel routers for on-chip networks," in *Proceedings of the 31st Annual International Symposium on Computer Architecture*, Munchen, Germany, June 19–23 2004.

[134] S. Murali, D. Atienza, L. Benini, and G. De Micheli, "A method for routing packets across multiple paths in NoCs with in-order delivery and fault-tolerance guarantees," *Hindawi VLSI Design*, vol. 2007, no. 37627, p. 11, May 2007.

[135] S. Murali, L. Benini, T. Theocharides, N. Vijaykrishnan, M. J. Irwin, and G. De Micheli, "Analysis of error recovery schemes for networks on chip," *IEEE Design and Test of Computers*, vol. 22, no. 5, pp. 434–442, September 2005.

[136] S. Murali, M. Coenen, A. Radulescu, K. Goossens, and G. De Micheli, "A methodology for mapping multiple use-cases onto networks on chips," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, Munich, Germany, March 06–10 2006.

[137] S. Murali and G. De Micheli, "Bandwidth-constrained mapping of cores onto NoC architectures," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, February 16–20 2004.

[138] S. Murali, P. Meloni, F. Angiolini, D. Atienza, S. Carta, L. Benini, G. De Micheli, and L. Raffo, "Designing application-specific networks on chips with floorplan information," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, California, November 05–09 2006.

[139] S. Murali, A. Mutapcic, D. Atienza, R. Gupta, S. Boyd, and G. De Micheli, "Temperature-aware processor frequency assignment for MPSoCs using convex optimization," in *Proceedings of the 5th IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Salzburg, Austria, September 30–October 03 2007.

[140] M. Newman, A.-L. Barabasi, and D. J. Watts, *The Structure and Dynamics of Networks*. Princeton University Press, 2006.

[141] C. A. Nicopoulos, D. Park, J. Kim, V. Narayanan, M. S. Yousif, and C. Das, "ViChaR: A dynamic virtual channel regulator for network-on-chip routers," in *Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture*, December 09–13 2006.

[142] E. Nilsson, M. Millberg, J. Oberg, and A. Jantsch, "Load distribution with the proximity congestion awareness in a network on chip," *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, vol. 1, March 03–07 2003.

[143] NIRGAM [Online]. Available: http://nirgam.ecs.soton.ac.uk/.

[144] Nostrum [Online]. Available: http://www.imit.kth.se/info/FOFU/Nostrum/.

[145] U. Y. Ogras, J. Hu, and R. Marculescu, "Key research problems in NoC design: A holistic perspective," in *Proceedings of the 3rd IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Jersey City, NJ, USA, September 19–21 2005.

[146] U. Y. Ogras and R. Marculescu, "Energy- and performance-driven NoC communication architecture synthesis using a decomposition approach," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, March 07–11 2005.

[147] U. Y. Ogras and R. Marculescu, "It's a small world after all: NoC performance optimization via long-range link insertion," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Special Section on Hardware/Software Codesign and System Synthesis, vol. 14, no. 7, pp. 693–706, July 2006.

[148] U. Y. Ogras and R. Marculescu, "Analytical router modeling for networks-on-chip performance analysis," in *Proceedings of Design, Automation and Test in Europe Conference (DATE)*, pp. 1096–1101, Nice, France, April 16–20 2007.

[149] U. Y. Ogras and R. Marculescu, "Analysis and optimization of prediction-based flow control in networks-on-chip," *ACM Transactions on Design Automation of Electronic Systems*, vol. 13, no. 1, January 2008.

[150] U. Y. Ogras, R. Marculescu, P. Choudhary, and D. Marculescu, "Voltage-frequency island partitioning for GALS-based networks-on-chip," in *Proceedings of the IEEE/ACM Design Automation Conference*, San Diego, June 2007.

[151] U. Y. Ogras, R. Marculescu, D. Marculescu, and E.-G. Jung, "Design and management of voltage-frequency island partitioned networks-on-chip," to appear in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Special Section on Networks-on-Chip, 2009.

[152] Orion [Online]. Available: http://www.princeton.edu/peh/orion.html.

[153] L. Ost, A. Mello, J. Palma, F. Moraes, and N. Calazans, "MAIA: A framework for networks on chip generation and verification," in *Proceedings of Asia South Pacific Design Automation Conference (ASPDAC)*, January 2005.

[154] G. Palermo and C. Silvano, "PIRATE: A framework for power/performance exploration of network-on-chip architectures," in *Proceedings of the 14th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Lecture Notes in Computer Science,* Springer, pp. 521–531, Santorini, Greece, September 15–17 2004.

[155] P. P. Pande, C. Grecu, M. Jones, A. Ivanov, and R. Saleh, "Performance evaluation and design trade-offs for network-on-chip interconnect architectures," *IEEE Transactions on Computers*, vol. 54, no. 8, pp. 1025–1040, August 2005.

[156] P. Pardalos and M. Resende, *Handbook of Applied Optimization.* Oxford University Press, 2002.

[157] P. M. Pardalos, F. Rendl, and H. Wolkowicz, "The quadratic assignment problem: A survey and recent developments," *Quadratic Assignment and Related Problems*, vol. 16, pp. 1–42, DIMACS Series in Discrete Mathematics and Theoretical Computer Science, 1994.

[158] K. Park and W. Willinger, *Self-Similar Network Traffic and Performance Evaluation.* Wiley Interscience, 1999.

[159] C. S. Patel, S. M. Chai, S. Yalamanchili, and D. E. Schimmel, "Power constrained design of multiprocessor interconnection networks," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 408–416, October 12–15 1997.

[160] K. Petersen and J. Oberg, "Toward a scalable test methodology for 2D-mesh network-on-chips," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, Nice, France, April 16–20 2007.

[161] D. Pham, S. Asano, M. Bolliger, M. N. Day, H. P. Hofstee, C. Johns, J. Kahle, A. Kameyama, J. Keaty, Y. Masubuchi, M. Riley, D. Shippy, D. Stasiak, M. Suzuoki, M. Wang, J. Warnock, S. Weitzel, D. Wendel, T. Yamazaki, and K. Yazawa, "The design and implementation of a first-generation CELL processor," *Proceedings of the International Solid-State Circuits Conference (ISSCC)*, vol. 1, pp. 184–592, February 10–15 2005.

[162] A. Pinto, L. P. Carloni, and A. L. Sangiovanni-Vincentelli, "Efficient synthesis of networks on chip," in *Proceedings of the 21st International Conference on Computer Design (ICCD)*, October 13–15 2003.

[163] A. Pinto, L. P. Carloni, and A. L. Sangiovanni-Vincentelli, "COSI: A framework for the design of interconnection networks," *IEEE Design and Test of Computers*, pp. 402–415, September/October 2008.

[164] P. Pop, P. Eles, T. Pop, and P. Zebo, "An approach to incremental design of distributed embedded systems," in *Proceedings of the 38th Conference on Design Automation (DAC)*, Las Vegas, Nevada, United States, June 2001.

[165] P. Poplavko, T. Basten, M. Bekooij, J. van Meerbergen, and B. Mesman, "Task-level timing models for guaranteed performance in multiprocessor networks-on-chip," in *Proceedings of the International Conference on Compilers, Architecture and Synthesis For Embedded Systems (CASES)*, San Jose, California, USA, October 30–November 01 2003.

[166] V. Puente, J. A. Gregorio, F. Vallejo, and R. Beivide, "Immunet: A cheap and robust fault-tolerant packet routing mechanism," in *Proceedings of the 31st Annual International Symposium on Computer Architecture*, pp. 198–209, June 19–23 2004.

[167] A. Pullini, F. Angiolini, D. Bertozzi, and L. Benini, "Fault tolerance overhead in network-on-chip flow control schemes," in *Proceedings of the 18th Annual Symposium on Integrated Circuits and System Design (SBCCI)*, Florianolpolis, Brazil, September 04–07 2005.

[168] G. Rangarajan and M. Ding, *Processes with Long-Range Correlations: Theory and Applications*. Berlin Heidelberg: Springer-Verlag, 2003.

[169] C. R. Reeves and J. E. Rowe, *Genetic Algorithms. Principles and Perspectives: A Guide to GA Theory*. Springer, 2003.

[170] C. Rhee, H. Y. Jeong, and S. Ha, "Many-to-many core-switch mapping in 2-D mesh NoC architectures," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 438–443, October 11–13 2004.

[171] S. M. Ross, *Simulation*. Academic Press, Second ed., 1997.

[172] J. Rossiter, *Model Based Predictive Control, A Practical Approach*. CRC Press, 2002.

[173] S. M. Sait and H. Youssef, *VLSI Physical Design Automation: Theory and Practice*. McGraw-Hill Inc, 1994.

[174] G. Salaun, W. Serwe, Y. Thonnart, and P. Vivet, "Formal verification of CHP specifications with CADP illustration on an asynchronous network-on-chip," in *Proceedings of the 13th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, March 12–14 2007.

[175] A. Schrijver, *Theory of Linear and Integer Programming*. John Wiley and Sons, 1998.

[176] D. Seo, A. Ali, W. Lim, N. Rafique, and M. Thottethodi, "Near-optimal worst-case throughput routing for two-dimensional mesh networks," in *Proceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA)*, June 04–08 2005.

[177] A. Shacham, K. Bergman, and L. P. Carloni, "The case for low-power photonic networks-on-chip," in *Proceedings of the 44th Annual Conference on Design Automation (DAC)*, San Diego, California, June 04–08 2007.

[178] L. Shang, L.-S. Peh, and N. K. Jha, "Dynamic voltage scaling with links for power optimization of interconnection networks," in *Proceedings of the 9th International Symposium on High-Performance Computer Architecture (HPCA)*, February 08–12 2003.

[179] L. Shang, L.-S. Peh, and N. K. Jha, "PowerHerd: Dynamically satisfying peak power constraints in interconnection networks," in *Proceedings of the ACM International Symposium on Supercomputing*, pp. 98–108, June 2003.

[180] L. Shang, L.-S. Peh, A. Kumar, and N. K. Jha, "Thermal modeling, characterization and management of on-chip networks," in *Proceedings of the 37th Annual IEEE/ACM International Symposium on Microarchitecture*, Portland, Oregon, December 04–08 2004.

[181] A. Sheibanyrad, I. M. Panades, and A. Greiner, "Systematic comparison between the asynchronous and the multi-synchronous implementations of a network-on-chip architecture," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, Nice, France, April 16–20 2007.

[182] B. Shim and N. R. Shanbhag, "Energy-efficient soft-error tolerant digital signal processing," *IEEE Transacions on Very Large Scale Integration Systems*, vol. 14, no. 4, pp. 336–348, April 2006.

[183] D. Shin and J. Kim, "Power-aware communication optimization for networks-on-chips with voltage scalable links," in *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, September 08–10 2004.

[184] D. Shin, J. Kim, and S. Lee, "Intra-task voltage scheduling for low-energy, hard real-time applications," *IEEE Design and Test*, vol. 18, no. 2, pp. 20–30, March/April 2001.

[185] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on soft error rate of combinational logic," in *Proceedings of the International Conference on Dependable Systems and Networks (DSN)*, June 23–26 2002.

[186] T. Simunic and S. Boyd, "Managing power consumption in networks on chip," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, March 04–08 2002.

[187] SONICS Smart Interconnects [Online]. Available: http://www.sonicsinc.com.

[188] V. Soteriou, H.-S. Wang, and L.-S. Peh, "A statistical traffic model for on-chip interconnection networks," in *Proceedings of the 14th IEEE International Symposium on Modeling, Analysis, and Simulation*, September 11–14 2006.

[189] K. Srinivasan and K. Chatha, "ISIS: A genetic algorithm based technique for custom on-chip interconnection network synthesis," in *Proceedings of the 18th International Conference on VLSI Design (VLSID) Held Jointly with 4th International Conference on Embedded Systems Design*, January 03–07 2005.

[190] K. Srinivasan and K. S. Chatha, "A technique for low energy mapping and routing in network-on-chip architectures," in *Proceedings of the 2005 International Symposium on Low Power Electronics and Design (ISLPED)*, San Diego, CA, USA, August 08–10 2005.

[191] K. Srinivasan and K. S. Chatha, "A low complexity heuristic for design of custom network-on-chip architectures," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, Munich, Germany, March 06–10 2006.

[192] K. Srinivasan, K. S. Chatha, and G. Konjevod, "Linear programming based techniques for synthesis of network-on-chip architectures," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 4, pp. 407–420, April 2006.

[193] S. Sriram and S. S. Bhattacharyya, *Embedded Multiprocessors: Scheduling and Synchronization*. Marcel Dekker Inc., 2002.

[194] S. Stuijk, T. Basten, M. Geilen, A. H. Ghamarian, and B. Theelen, "Resource efficient routing and scheduling of time-constrained streaming communication on networks-on-chip," *Journal of Systems Architecture: The EUROMICRO Journal*, vol. 54, no. 3–4, March 2008.

[195] S. Stuijk, M. Geilen, and T. Basten, "Throughput-buffering trade-off exploration for cyclo-static and synchronous dataflow graphs," *IEEE Transactions on Computers*, vol. 57, no. 10, p. 28, October 2008.

[196] C. Sun, L. Shang, and R. P. Dick, "Three-dimensional multi-processor system-on-chip thermal optimization," in *Proceedings of the 5th IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 117–122, Salzburg, Austria, September 30–October 03 2007.

[197] H. Takagi, *Queueing Analysis — A Foundation of Performance Evaluation*. North-Holland: Elsevier, 1991.

[198] M. B. Taylor, J. Kim, J. Miller, D. Wentzlaff, F. Ghodrat, B. Greenwald, H. Hoffman, P. Johnson, W. Jae-Wook Lee Lee, A. Ma, A. Saraf, M. Seneski, N. Shnidman, V. Strumpen, M. Frank, S. Amarasinghe, and A. Agarwal, "The Raw microprocessor: A computational fabric for software circuits and general purpose programs," *IEEE Micro*, vol. 22, no. 2, pp. 25–35, March/April 2002.

[199] C. Teuscher, "Nature-inspired interconnects for self-assembled largescale network-on-chip designs," *Chaos: An Interdisciplinary Journal of Nonlinear Science*, vol. 17, no. 2, pp. 26–106, 2007.

[200] J. W. van den Brand, C. Ciordas, K. Goossens, and T. Basten, "Congestion-controlled best-effort communication for networks-on-chip," in *Proceedings of Design Automation and Test in Europe Conference (DATE)*, April 2007.

[201] S. Vangal, J. Howard, G. Ruhl, S. Dighe, H. Wilson, J. Tschanz, D. Finan, P. Iyer, A. Singh, T. Jacob, S. Jain, S. Venkataraman, Y. Hoskote, and N. Borkar, "An 80-Tile 1.28TFLOPS network-on-chip in 65nm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference (ISSCC)*, February 2007.

[202] G. Varatkar and R. Marculescu, "On-chip traffic modeling and synthesis for MPEG-2 video applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 1, pp. 108–119, January 2004.

[203] G. Varatkar, S. Narayanan, N. R. Shanbhag, and D. L. Jones, "Trends in energy-efficiency and robustness using stochastic sensor network-on-a-chip," in *Proceedings of the 18th ACM Great Lakes Symposium on VLSI*, Orlando, Florida, USA, May 04–06 2008.

[204] H. Wang, L.-S. Peh, and S. Malik, "Power-driven design of router microarchitectures in on-chip networks," in *Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture*, December 03–05 2003.

[205] H. Wang, L.-S. Peh, and S. Malik, "A technology-aware and energy-oriented topology exploration for on-chip networks," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, March 07–11 2005.

[206] H. Wang, X. Zhu, L.-S. Peh, and S. Malik, "Orion: A power-performance simulator for interconnection networks," in *Proceedings of the 35th Annual International Symposium on Microarchitecture*, pp. 294–305, November 2002.

[207] D. J. Watts, *Small Worlds: The Dynamics of Networks Between Order and Randomness*. Princeton, NJ: Princeton University Press, 1999.

[208] Wormsim [Online]. Available: http://www.ece.cmu.edu/∼sld/.

[209] F. Xue and P. R. Kumar, "Scaling laws for ad-hoc wireless networks: An information theoretic approach," *Foundations and Trends in Networking, Now Publishers Inc.*, vol. 1, no. 2, pp. 145–270, 2006.

[210] T. T. Ye, L. Benini, and G. De Micheli, "Analysis of power consumption on switch fabrics in network routers," in *Proceedings of the 39th Conference on Design Automation (DAC)*, pp. 524–529, New Orleans, Louisiana, USA, June 10–14 2002.

[211] T. T. Ye and G. De Micheli, "Physical planning for multiprocessor networks and switch fabrics," in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 97–107, June 2003.

[212] Z. Yu and B. Baas, "Implementing tile-based chip multiprocessors with GALS clocking styles," in *Proceedings of the International Conference on Computer Design*, pp. 174–179, October 2006.

[213] D. Zhao and Y. Wang, "SD-MAC: Design and synthesis of a hardware-efficient collision-free QoS-aware MAC protocol for wireless networks-on-chip," *IEEE Transactions on Computers*, vol. 57, no. 9, pp. 1230–1245, May 2008.

[214] E. Zitzler, M. Laumanns, and L. Thiele, "SPEA2: Improving the strength pareto evolutionary algorithm," *Evolutionary Methods for Design, Optimization and Control with Applications to Industrial Problems*, pp. 95–100, Greece, Athens 2001.