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# The Predictive Technology Model in the Late Silicon Era and Beyond

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# The Predictive Technology Model in the Late Silicon Era and Beyond

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## Abstract

The aggressive scaling of CMOS technology has inevitably led to vastly increased power dissipation, process variability and reliability degradation, posing tremendous challenges to robust circuit design. To continue the success of integrated circuits, advanced design research must start in parallel with or even ahead of technology development. This new paradigm requires the Predictive Technology Model (PTM) for future technology generations, including nanoscale CMOS and post-silicon devices. This paper presents a comprehensive set of predictive modeling developments. Starting from the PTM of traditional CMOS devices, it extends to CMOS alternatives at the end of the silicon roadmap, such as

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strained Si, high-k/metal gate, and FinFET devices. The impact of process variation and the aging effect is further captured by modeling the device parameters under the influence. Beyond the silicon roadmap, the PTM outreaches to revolutionary devices, especially carbon-based transistor and interconnect, in order to support explorative design research. Overall, these predictive device models enable early stage design exploration with increasing technology diversity, helping shed light on the opportunities and challenges in the nanoelectronics era.

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# Glossary

| | |
|---|---|
| Channel doping: | the equivalent doping concentration in the channel region to determine the threshold voltage. |
| CMOS: | complementary metal-oxide-semiconductor field-effect transistor. |
| CNT: | carbon nanotube based devices. Depending on the chirality, CNT is either metallic or semiconducting. |
| DIBL: | drain induced barrier lowering. |
| Equivalent oxide thickness: | the equivalent gate oxide thickness that considers the quantum effect and poly-depletion. |
| FinFET: | a double gate device that has better control of short-channel effects than traditional MOSFET devices. |
| Predictive Technology Model: | compact models that predict future device performance before the corresponding technology is mature. |

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| | |
|---|---|
| Process variation: | fluctuations in device parameters that are induced by random uncertainties or the manufacturing process. |
| Reliability degradation: | temporal change of device performance, which is a function of technology parameters and operation conditions. |
| Short-channel effects: | the modification of carrier transport and the threshold voltage when the channel length is reduced to the sub-micron regime. |
| Strained Si: | the process techniques to stretch the silicon atoms beyond their normal interatomic distance. |
| Surface potential: | the electrostatic potential on the surface of the channel. |
| Technology scaling: | a systematic approach to miniaturize the device for better performance. |
| Threshold voltage: | the specific value of gate voltage when a MOSFET switches into the strong-inversion region. |
| Velocity overshoot: | the velocity exceeds the saturation velocity when the channel length is comparable to or shorter than the mean-free-path of a carrier. |
| Velocity saturation: | the carrier velocity reaches the maximum when the electric field is strong enough. |
| Verilog-A: | a standard modeling language to describe the analog behavior. |
| NBTI: | negative bias temperature instability, which is more pronounced in PMOS devices. |

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# 1

## Introduction

The minimum feature size of CMOS technology is expected to reach 10 nm in 10 years [51]. Beyond that benchmark, the present scaling approach may have to take a different route to overcome dramatic barriers in power consumption, process and environmental variations, and temporal reliability degradation. The grand challenge to the integrated circuit (IC) community is to identify unconventional materials and structures, such as carbon-based electronics, integrate them into the circuit architecture, and enable continuous growth of chip scale and performance [17, 51]. The Predictive Technology Model (PTM), which bridges the process/material development and circuit simulation through compact device modeling, is essential to assessing the potential and limits of new technologies and to supporting early design prototyping.

Predictive models of electron devices are the critical interface between technology innovation and IC design exploration, as shown in Figure 1.1. Compatible with circuit simulation tools, they significantly improve design productivity, providing the insight into the relationship between technology/design choices and circuit performance. Different from traditional compact models (e.g., BSIM), PTM uses a simple set of physical equations that capture the essential behavior of charge and

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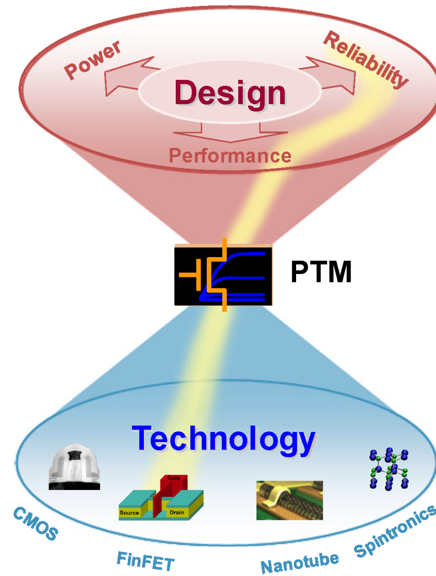


Fig. 1.1 PTM: a bridge between technological prediction and early stage design exploration.

carrier transport. The electrostatic models emphasize the dependence of the threshold voltage on physical aspects of the device like channel length, channel doping, HALO implant, etc. The transport part of the model adopts the velocity saturation model with overshot behavior. In order to guarantee the quality of the prediction, PTM should be scalable with latest technology advances, accurate across a wide range of process uncertainties and operation conditions, and efficient for large-scale computation. As semiconductor technology scales into the nanoscale regime, these modeling demands are tremendously challenged, especially by the introduction of alternative device materials and structures, as well as the ever-increasing amount of process variations.

This paper presents a comprehensive review of the development and latest results of the Predictive Technology Model for nanoscale devices, covering end-of-the-roadmap and post-silicon technologies. Driven by the increasingly complex and diverse nature of the underlying technology, the overarching goal of PTM is to provide early comprehension of process choices and design opportunities, as well as to address key

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design needs, such as variability and reliability, for robust system integration. This paper presents four specific topics on predictive modeling challenges, ranging from conventional CMOS scaling, alternative technologies that enhance nominal CMOS performance, variability and reliability issues at the end of the roadmap, to emerging devices beyond the Si roadmap:

- *Predictive modeling of conventional CMOS technology* (*Section 2*): CMOS will arguably be the technology of choice for the next 15 years. To predict future technology characteristics, an intuitive approach would simply scale down the feature size and voltage parameters, such as supply voltage and threshold voltage ($V_{\mathrm{th}}$), from an existing technology. However, this approach is overly simplified and underestimates the overall device performance toward the end of the roadmap [128]. During technology scaling, process developers will optimize many other aspects of the device beyond sole geometry scaling. For instance, the scaling of $V_{\mathrm{th}}$ not only requires the change of channel doping concentration, but also impacts other physical parameters, such as mobility, saturation velocity, and the body effect. These intrinsic correlations among physical parameters need to be carefully considered for an accurate prediction.
- *PTM for alternative materials and structures* (*Section 3*): the scaling of traditional bulk CMOS structure is slowing down in recent years as fundamental limits are rapidly approached. For instance, short-channel effects, such as drain-induced-barrier-lowering (DIBL) and threshold voltage rolloff, severely increase leakage current and degrade the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio. To overcome these difficulties and continue the path projected by Moore's law, new materials (e.g., strained silicon, metal gate, high-k dielectrics, low-resistance source/drain) and structures (e.g., double-gate device) need to be adopted into conventional CMOS technology. Therefore, predictive models for bulk CMOS technology should be updated to capture the distinct electrical behavior of

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these advances, guaranteeing state-of-the-art predictions and design benchmarking toward the 10nm regime.

- *Modeling of variability and reliability effects (Section 4)*: while technology scaling can be extended with alternative materials and structures, CMOS technology will eventually reach the ultimate limits that are defined by both physics and the fabrication process. One of the most profound physical effects will result from the vastly increased parameter variations and reliability degradation due to manufacturing and environmental factors. These parameter fluctuations lead to excessive design margins, degrade the yield, and invalidate the deterministic design methodologies currently used in industry. To maintain design predictability with such extremely scaled devices, predictive models should incorporate both static process variations and temporal shift of device parameters. They should be extended from the traditional corner-based approach to a suite of modeling efforts, including extraction methods, the decoupling of variation sources, and highly efficient strategies for the statistical design paradigm.
- *Predictive modeling of post-silicon devices* (*Section 5*): beyond the far end of the CMOS technology roadmap, several emerging technologies have been actively researched as alternatives, such as nano-tubes, nano-wires, and molecular devices. As demonstrated in the success of PTM for CMOS, the outreach of PTM to these revolutionary technologies will help shed light on design opportunities and challenges with post-silicon technologies beyond the 10 nm regime.

Predictive models for CMOS devices and their variability are built upon standard compact models. They are ready to be integrated into circuit simulation tools. For nanoelectronic devices, PTM employs Verilog-A for the implementation; it plays an essential role in joint technology-design exploration. Solutions to those predictive modeling challenges will ensure a timely and smooth transition from CMOS-based design to robust integration with post-silicon technologies.

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