
**System-in-Package:
Electrical and Layout
Perspectives**

System-in-Package: Electrical and Layout Perspectives

Lei He

*University of California, Los Angeles, USA
lhe@ee.ucla.edu*

Shauki Elassaad

*Stanford University, USA
shauki@stanford.edu*

Yiyu Shi

*Missouri University of Science and Technology, USA
yshi@mst.edu*

Yu Hu

*University of Alberta, CANADA
bryanhu@ece.ualberta.ca*

Wei Yao

*University of California, Los Angeles, USA
weiyao@ee.ucla.edu*

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System-in-Package: Electrical and Layout Perspectives

Lei He¹, Shauki Elassaad², Yiyu Shi³,
Yu Hu⁴ and Wei Yao⁵

¹ *University of California, Los Angeles, CA 90095, USA, lhe@ee.ucla.edu*

² *Stanford University, Stanford, CA 94305, USA, shauki@stanford.edu*

³ *Missouri University of Science and Technology, Rolla, MO 65409, USA, yshi@mst.edu*

⁴ *University of Alberta, Edmonton, Alberta T6G 2R3, CANADA, bryanhhu@ece.ualberta.ca*

⁵ *University of California, Los Angeles, CA 90095, USA, weiyao@ee.ucla.edu*

Abstract

The unquenched thirst for higher levels of electronic systems integration and higher performance goals has produced a plethora of design and business challenges that are threatening the success enjoyed so far as modeled by Moore's law. To tackle these challenges and meet the design needs of consumer electronics products such as those of cell phones, audio/video players, digital cameras that are composed of a number of different technologies, vertical system integration has emerged as a required technology to reduce the system board space and height in addition to the overall time-to-market and design cost. System-in-package (SiP) is a system integration technology that achieves the aforementioned needs in a scalable and cost-effective way, where

multiple dies, passive components, and discrete devices are assembled, often vertically, in a package. This paper surveys the electrical and layout perspectives of SiP. It first introduces package technologies, and then presents SiP design flow and design exploration. Finally, the paper discusses details of beyond-die signal and power integrity and physical implementation such as I/O (input/output cell) placement and routing for redistribution layer, escape, and substrate.

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1

Introduction

Since birth of the integrated circuit (IC), the ever-increasing integration level has been enabling more functions at reduced cost. This has been primarily driven by Moore's Law, which dictates the scaling of a single chip in the past half-century. On top of this, at the system integration level, technologies such as wafer-scale integration and multi-chip modules (MCM) have been explored to further increase the design size and reduce the cost. Today, with the growing scalability of semiconductor processes, the higher level of functional integration at the die level, and the system integration of different technologies needed for consumer electronics, system-in-package (SiP) is the new advanced system integration technology, which integrates (or vertically stacks) within a single package multiple components such as CPU, digital logic, analog/mixed signal, memory, and passive and discrete components in a single system.

SiP reduces the form factor of a system. Compared with system-on-a-chip (SoC), SiP decreases the cost due to the following reasons. First, different components may be fabricated in different generations or different types of technologies, without complications and high cost associated with integrating heterogeneous technologies in one process.

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Second, the same component can be fabricated in a large volume and used for different systems, amortizing the ever-increasing non-recurring engineering expenses such as those for designing and mask. Finally, the size of each individual die of the SiP is much smaller than the size of the chip if SoC is used for the same system. Smaller size improves yield rate and reduces production cost. It also makes design easier and reduces time-to-market.

While SiP clearly has advantages, the design complexities and costs associated with designing the package and integrating the different components in a system may eclipse the design challenges of the stand-alone dies. Packaging has evolved over the years from the point where chips had few pins to designs that have thousands of pins. Traversing the evolution of the electronic packaging, different technologies have been designed and adopted to solve the design and cost problems associated with the ever-increasing number of I/Os. Electronic packaging has started with dual-in-line package (DIP), and evolved to include a variety of technologies such as tape-automated bonding (TAB), pin grid array (PGA), ball grid array (BGA), and many other forms of system outline packages (SOP) and chip-scale packages (CSP). SiP with multiple dies and passive components in one package introduces more design challenges than CSP.

This survey focuses on electrical and layout perspectives of SiP, without discussing thermal and mechanic characteristics of SiP. In addition, this survey does not consider three-dimensional (3D) integration using through-silicon vias (TSVs). The remainder of the survey is organized as follows. Section 2 presents a tutorial on IC package, and Section 3 introduces overall design challenges and design exploration of SiP with consideration of beyond-die power and signal integrity, and Section 4 presents placement and routing for SiP.

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