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# Manufacturability Aware Routing in Nanometer VLSI

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## Abstract

This monograph surveys key research challenges and recent results of manufacturability aware routing in nanometer VLSI designs. The manufacturing challenges have their root causes from various integrated circuit (IC) manufacturing processes and steps, e.g., deep sub-wavelength lithography, random defects, via voids, chemical–mechanical polishing, and antenna effects. They may result in both functional and parametric yield losses. The manufacturability aware routing can be performed at different routing stages including global routing, track routing, and detail routing, guided by both manufacturing process models and manufacturing-friendly rules. The manufacturability/yield optimization can be performed through both correct-by-construction (i.e., optimization during routing) and construct-by-correction (i.e., post-routing optimization). This monograph will provide a holistic view of key design for manufacturability issues in nanometer VLSI routing.

# Contents

# 1

# Introduction

Nanometer very large scale integrated (VLSI) circuit design faces tremendous challenges due to the manufacturing limitations. These manufacturing and process related challenges include the printability issues due to deep sub-wavelength lithography, the topography variations due to chemical–mechanical polishing (CMP), the random defects due to missing or extra material, and so on. Thus, the conventional design "closure" (on timing/noise, etc.) may not automatically guarantee the manufacturing closure due to the manufacturing yield loss. Manufacturability aware layout optimization plays a key role in the overall yield improvement.

In this monograph, we survey key aspects of manufacturability issues and how to alleviate them during the routing stage. There have been some design-for-manufacturability (DFM) efforts in earlier design stages such as logic synthesis and placement [41, 46, 89], yet routing is often considered one of the most critical stages in addressing the manufacturability issues due to the following reasons [24, 25, 26, 47, 86]: (1) many key manufacturing issues (e.g., topography variation due to chemical–mechanical polishing — CMP, random defects, printability due to optical lithography limitations, and so on) are tightly coupled

with interconnects/wires which are mainly determined by routing; (2) routing is the last major VLSI physical design step before manufacturing, thus it has comprehensive picture of the physical layout needed to accurately estimate the overall manufacturability; (3) during routing it still has considerable flexibility to optimize and trade-off manufacturability and other conventional design objectives (e.g., timing, noise, power). These factors have led to very active academic and industrial research and development in *manufacturability aware routing*, which is the focus of this monograph.

The rest of the monograph will be organized as follows. Section 1 gives an overview of major manufacturability issues in nanometer VLSI designs, reviews the routing basics, and discusses various approaches to deal with manufacturability in routing. Then from Section 2 to Section 6, key manufacturability issues due to various process limitations will be discussed and dealt with through different manufacturability aware routing techniques, including CMP aware routing (Section 2), random-defect aware routing (Section 3), lithography aware routing (Section 4), redundant via aware routing (Section 5), and antenna-effect aware routing (Section 6). In Section 7, some more issues in manufacturability aware routing such as dealing with multiple DFM objectives and complicated design rules will be discussed, followed by summary and concluding remarks in Section 8.

## 1.1 Major Manufacturability Issues

In this section, we give an overview of major manufacturing issues which affect yield in nanometer designs (e.g., 65 nm technology node and below) [32, 100], and analyze their causes and effects, such as (1) printability issues due to sub-wavelength lithography system (i.e., feature size much smaller than the optical wavelength); (2) random defects due to missing or extra material; (3) topography variations due to chemical–mechanical polishing (CMP), and (4) other causes such as via failure and antenna effects.

(1) A fundamental limitation for the *sub-wavelength optical lithography* is WYSINWYG, i.e., "what you see (at design) is not what you get (at fab)". The printability issue arises between neighboring wires/vias

due to sub-wavelength effects and process variations. As of today, the 193 nm wavelength optical lithography is still the dominant integrated circuit manufacturing process for 45 nm and 32 nm nodes. It is likely to remain so for 22 nm node or even below [106] due to delay in other viable next-generation lithography (e.g., extreme ultra-violet lithography — EUVL) and continued industry push in extending the 193 nm lithography through immersion lithography, resolution enhancement techniques (RET), and so on. However, if the initial design is very litho-unfriendly, even aggressive RET may not be able to solve the printability problem. Thus, the routing tool needs to construct litho-friendly and printable layouts.

As technology is further scaled down below 32 nm, the current single exposure immersion lithography is hit by the theoretical limit on feature resolution. As a candidate solution, EUVL with 13.5 nm wavelength has been researched heavily, targeting sub-32 nm technology nodes. However, the deployment of EUVL for commercial volume production has been delayed multiple times (due to light sources, material issues, mask fabrication, and so on), and is likely to be pushed out to the 16 nm node or below, if at all [33, 56, 62]. To bridge the gap between the current single exposure immersion lithography and EUV lithography, double patterning lithography (DPL) has received a lot of attention from industry. DPL is regarded as a technically and practically viable technology to achieve high resolution for 22 nm node [2, 49, 53, 62, 96, 104, 128]. However, the deployment of DPL needs to tackle two major challenges, layout decomposition and overlay error [2, 33, 56, 107], and routing and layout optimization can play a proactive role to mitigate them.

(2) Smaller feature size makes nanometer VLSI designs more vulnerable to *random defects*, which can be further divided into open or short defects [31, 61]. The back-end-of-line (BEOL) defects [57] may cause electrical opens or shorts on the interconnects. While it is generally believed that the yield loss due to systematic sources is greater than that due to random defects during the technology and process ramp-up stage, the systematic yield loss can be largely eliminated when the process becomes mature and systematic variations are ultimately compensated. On the other hand, the random defects which are inherent due to manufacturing limitations will still be there even for mature

fabrication process. Thus, its relative importance will indeed be bigger for mature process with systematic variations designed in [25].

(3) *Topography (thickness) variation* due to dishing and erosion after CMP is shown to be systematically determined by wire density distribution [37, 66, 101, 122, 142]. Even after CMP, intra-chip topography variation can still be in the order of 20–40% [42, 101]. Such topography variation leads to not only significant performance degradation due to increased wire resistance, but also acute manufacturing issues like etching and printability due to defocus [37, 42, 101, 122]. The main reason for the copper CMP problems is uneven wire density distribution. Higher wire density usually leads to copper thickness reduction due to erosion after CMP [66, 142], making resistance worse. Also, the reduced copper thickness after CMP can worsen the scattering effect, further increasing resistance [52]. The wire density distribution is directly affected by routing.

(4) Vias may fail due to various reasons such as random defects, electromigration, cut misalignment, and/or thermal stress-induced voiding effects. Redundant vias (or double vias) can be inserted during VLSI routing to make the vias more robust [134]. Redundant via insertion is known to be highly effective, leading to 10–100× lower failure rate [11].

(5) During IC fabrication process, charges from plasma etching can be accumulated in long floating wires. Such charges may result in high currents to thin-oxide gates (i.e., Fowler-Nordheim tunneling current), and cause permanent damages to the gates. This is known as the *antenna effect* [82]. There are three kinds of solutions to resolve the antenna effect: protection diode embedding, diode insertion after placement and routing, and jumper insertion. While the first two solutions need extra area for diode, the jumper insertion incurs overhead in routing system due to additional vias [18].

These nanometer manufacturing issues will be addressed in manufacturability aware VLSI routing.

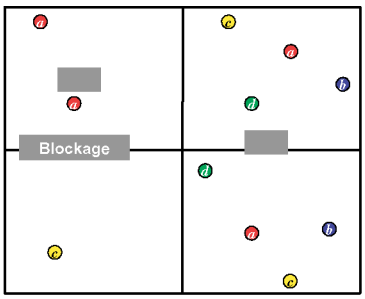
## 1.2 VLSI Routing Basics

Routing is a key step in integrated circuit physical design to connect signal nets together through geometrical embedding after block/cell

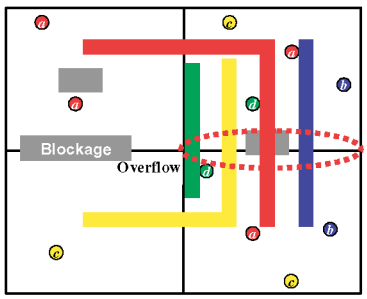
placement. Due to the complexity of routing, divide-and-conquer approach is usually used to make the problem size manageable, e.g., through global routing and detailed routing. Global routing divides the chip into global routing cells and plans approximate routing paths for global nets (i.e., the signal nets between different routing cells). Detailed routing follows the guidance from global routing and finalizes the exact geometrical embedding/routing for all nets while satisfying all the design rule checking (DRC). Track routing, as an intermediate step between global and detailed routing, can expedite detailed routing by embedding major trunks from each net within a panel (a row/column of global routing cells) in DRC-friendly manner [4].

Figure 1.1 illustrates an example of modern routing systems [22, 23, 35, 73, 87, 91, 94, 103]. The input to the routing system is the legalized placement result where pins are not yet connected. The entire chip area is further dissected into global routing grid in order to reduce routing complexity as shown in Figure 1.1(a). Once partitioned properly into routing grids, the goal of global routing is to find a grid-to-grid routing path instead of pin-to-pin connection for each net. One possible global routing solution is shown in Figure 1.1(b). However, such solution could cause routing to be heavily congested and even unroutable. An alternative global routing solution is shown in Figure 1.1(c) where wires are more evenly distributed without any overflow [59, 127].

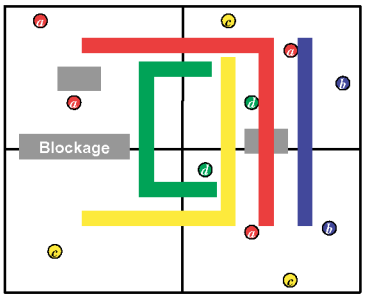
Once a global routing solution is fixed, track routing tunes the locations of wire pieces such that the wires can be more DRC friendly (e.g., connected to the pins, minimum spacing rules, and so on), while honoring the global routing decisions [4]. An example of track routing is shown in Figure 1.1(d) where wire pieces are placed such that maximum number of pins can be connected. Detailed routing follows the track routing solution to finalize all the electrical connections. Mainly, it performs local wiring to connect pins to wires (from track routing) as shown in Figure 1.1(e), or pins to pins for short wires (which are not considered during global routing) as in Figure 1.1(f). The final detailed routing solution should not have any electrical open or short in a DRC-clean manner. For difficult designs, these steps may need to be repeated in order to satisfy multiple design constraints (e.g., timing, power, noise, and so on) and reach the design closure.



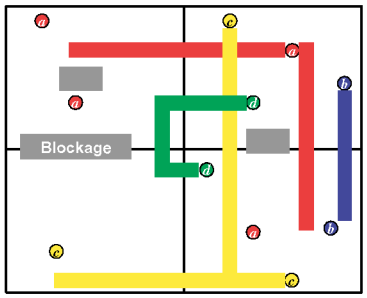

(a) After placement, the chip area is divided into global routing cells, with routing blockages in grey and four nets, *a, b, c*, and *d*.



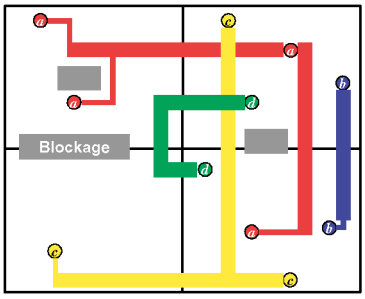

(b) A global routing solution where each net is routed in the shortest path, causing overßow (too many wires in a small region).



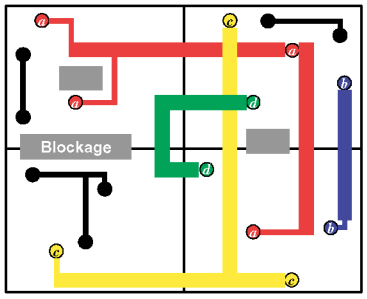

(c) The overflow is removed by altering the routing path of net *d* with more wirelength, which is the output from global routing.




(d) Track routing tunes the location of each segment in a way that the distance from the corresponding pins is minimized, avoiding routing blockages.




(e) Detailed routing connects a pin to the nearest wire for each net in a DRC clean manner.




(f) Detailed routing also completes local nets within each global routing grid.

Fig. 1.1 Illustration of a modern routing system which consists of three routing stages: global routing, track routing, and detailed routing.

As seen from Figure 1.1, each routing stage has information on wire distribution, connectivity, and so on but at different levels of accuracy. For example, wire density distribution can be estimated as early as global routing with a high accuracy, and the spacing between majority of wires may be known during track routing. However, detailed wire shapes will be finalized only during detailed routing.

Depending on how a router places polygon shapes, a router can be classified into either *grid-based* routing or *gridless* routing [105]. In a grid-based routing system, polygons like vias or wires need to follow the underlying routing grid, thus only discrete wire widths and spacings such as 1×, 2×, 3×, and so on are available. A gridless router does not assume any underlying grid but directly manipulates the polygon shapes using some tile graph, thus it can have arbitrary width or spacing as long as the design rules are satisfied. In general, grid-based routing is more popular due to regular wire width, wire spacing, and faster runtime. On the other hand, gridless routing has more flexibility and solution space due to variable width and spacing. Thus, it could potentially achieve better solution quality. But the router complexity and runtime may be significantly higher [15, 30]. In a modern routing systems, a hybrid approach may be adopted, or a finer subgrid could be used to mimic a gridless router [75].

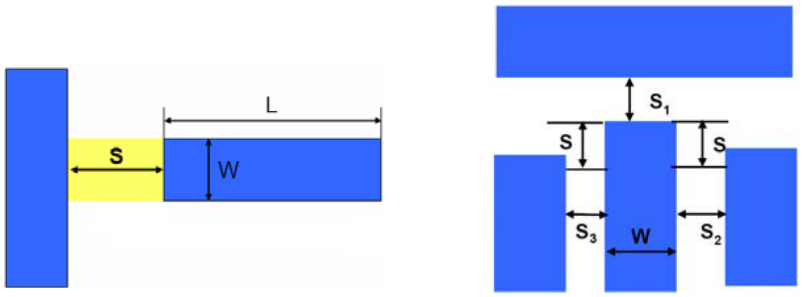
## 1.3 Rule vs. Model-Based Manufacturability Aware Routing

The approaches for manufacturing aware routing can be roughly classified into two groups: *rule-based* and *model-based*. The rule-based approach imposes additional manufacturability-driven design rules on a router to avoid manufacturability-unfriendly patterns. The model-based approach utilizes some chip manufacturing process models to estimate the manufacturability/yield and guide the router. There are pros and cons for both rule-based and model-based approaches in terms of runtime, scalability, implementation, controllability, trade-off, etc.

Rule-based approach extends the conventional *design rules* paradigm, by imposing a new set of manufacturability friendly design rules provided by the fab. These new manufacturability aware rules can be *required/hard* rules, or *recommended/soft* rules. Since existing

routing systems have been based on design rules for decades [85], the rule-based approach is friendly to the conventional design flow, which makes it seemingly easy to implement and apply. However, there are several serious challenges with rule-based approach.

(1) The number of such manufacturability aware rules is increasing exponentially with the introduction of each new technology node. For example, while the number of rules is only a few dozen at 180 nm node, it reaches to several hundreds at 65 nm node.
(2) The complexity of ensuring these rules becomes more computationally expensive, as the rules are becoming more complicated and increasingly context-sensitive [29, 32, 74]. For example, the minimum spacing between wires may depend on the wire lengths and the neighborhood wires, as shown in an example in Figure 1.2. Therefore, simply checking




(a) (b)

| Description | Rule (μm) |
|---|---|
| Minimum spacing (S) between a metal and the end-of-line of the metal whose edge width (W) ≤ 0.2 μm | 0.14 |
| If a metal of width (W) ≤ 0.2 has neighboring metals along three adjacent edges, then one of the spacings ($S_1$ or $S_2$ or $S_3$) should be ≥0.14 μm | 0.14 |
| Otherwise, minimum spacing | 0.11 |

Fig. 1.2 A context-dependent minimum spacing rule in a 65 nm technology is shown [29]. There are more and more complicated rules like this in sub-65 nm designs.

rules would need considerable amount of computing resource. More examples of how to deal with these rules will be discussed in Section 7.2.

(3) The rules are binary in nature, i.e., either following the rule or violating the rule, thus the rule-based approach does not provide smooth trade-off among different design objectives, such as timing, noise, area, and manufacturability.

(4) The rules may be too restrictive and pessimistic. Sometimes, it may be infeasible to achieve the area or performance goal due to large guard-bands from these rules. For this reason, the restrictive design rules (RDR) [76, 77, 98, 129], which are widely used for transistor/poly layout, are not widely adopted for routing, as routing patterns can be extremely complicated. Furthermore, the rules themselves may not be accurate enough to model very complicated manufacturing processes, in particular for the future deeper sub-wavelength lithography processes.

Due to these limitations of the rule-based approach, there have been significant research efforts in the model-based manufacturability aware routing recently, expecting that models will capture the overall manufacturability more accurately and holistically at affordable computational overhead. A modern IC manufacturing system involves non-linear optical, chemical, electrical, and mechanical processes which could be extremely complicated to model accurately and efficiently. For example of lithography, the model needs to capture the process where light source will pass through a mask and react with photoresists on the wafer surface, and result in printed images. There are process variations involved, and various resolution enhancement techniques may be used. The challenge with model-based approach is how to abstract a set of reasonably accurate and high-fidelity models at various abstraction levels to guide physical layout optimizations. Meanwhile, the models have to be compact and efficient enough to be embedded in the already time-consuming VLSI routing system. Therefore, a key technical bottleneck

for model-based manufacturability aware routing is to develop simple yet high-fidelity models, and apply them at proper routing stages in a seamless manner with consideration of other routing objectives. The model-based approach can be coupled with a small set of required design rules.

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