Radiation-induced Soft Errors: A Chip-level Modeling Perspective

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Norbert Seifert

Intel Corporation
Logic Technology Development Q&R
Hillsboro, OR 97124
USA

norbert.seifert@intel.com

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Norbert Seifert

Intel Corporation, Logic Technology Development Q&R, Hillsboro, OR 97124, USA, norbert.seifert@intel.com

Abstract

Chip-level soft-error rate (SER) estimation can come from two sources: direct experimental measurement and simulation. Because SER mitigation decisions need to be made very early in the product design cycle, long before product Si is available, a simulation-based methodology of chip-level radiation-induced soft error rates that is fast and reasonably accurate is crucial to the reliability and success of the final product.

The following contribution summarizes selected publications that are deemed relevant by the author to enable a truly chip-level radiation-induced soft error rate estimation methodology. Although the strategies and concepts described have microprocessors manufactured in bulk CMOS technologies in mind, there is no fundamental reason why they cannot be applied to other technologies and different types of integrated circuits (ICs).

Contents

1 Introduction **1**

1.1 SER Fundamentals 2
1.2 Particle-induced Soft Error Upset Modes 4
1.3 The Unit of SER 8
1.4 System-level Error Types 8

2 The Physics of Soft Errors in a Terrestrial Radiation Environment **11**

2.1 Charge Generation and Collection Process 11
2.2 The Terrestrial Radiation Environment 13

3 SER Trends **25**

3.1 Nominal SBU SER Trends 25
3.2 MCU Trends 30
3.3 Combinational Logic SER Trends 33
3.4 Redundancy-hardened Device SER Trends 36

4 SER Modeling Approaches **39**

4.1 Accuracy Considerations 39
4.2 Nominal SBU Modeling 42
4.3 Timing Vulnerability Factor (TVF) Modeling 61
4.4 SER Simulations of Static Combinational Logic 67

4.5 Architectural Vulnerability Factors (AVF) Modeling 81
4.6 A Circuit-level Simulation Strategy of Radhard Devices that Utilize Redundancy 86
4.7 Modeling of MBU in Memory Arrays 93
4.8 Chip-level SER Rollup: Putting it all together 97

Acknowledgments **101**

A Appendices **103**

A.1 Appendix 1 — Selected Acronyms 103
A.2 Appendix 2 — Selected Online Resources 104
A.3 Appendix 3 — Alternative SEU Models 104
A.4 Appendix 4 — A simple SER Compact Model 108
A.5 Appendix 5 — A Compact Model that accounts for Charge Sharing 110

References **115**

1

Introduction

This work summarizes the modeling and technology related content of a series of one day tutorials given at several major conferences during 2006–2008 by Norbert Seifert, Subhasish Mitra and Pia Sanda. The tutorials provided an overview of key single event (SE) phenomena, discussed the impact of technology scaling on soft error rates, introduced the basic concepts of modeling of soft errors, covered well-known as well as novel mitigation techniques and presented actual system behavior data in the presence of soft errors for selected case studies. In these tutorials Dr. Seifert covered all technology and circuit-level aspects of soft errors, while most mitigation techniques were introduced by Prof. Mitra. Results of case studies of soft errors in real systems were presented and discussed by Dr. Sanda. Due to the distinct nature of the topics covered and because each presenter solely owned the content of his or her presentation, it was decided to have this separation preserved in the current edition of FTEDA. The author of this work included key publications published after 2008 and further added content and references that were not covered in the tutorials due to the limited time available.

After introducing the key strategy for modeling chip-level soft error rates (SER) used throughout this work in Section 1.1, important types of single-event phenomena are discussed in Section 1.2. Mainly radiation-induced phenomena that result in soft errors, i.e., upsets that do not cause permanent damage, are being considered in this work. The terrestrial particle environment and charge generation and collection processes are addressed in Section 2. SER trends of key SER contributors are summarized in Section 3. SER modeling methods are discussed in Sections 4.2–4.7. Finally, Section 4.8 illustrates how all components can be put together in a truly chip-level capable SER strategy and tool.

1.1 SER Fundamentals

1.1.1 System-level SER Modeling Strategy Overview

"*Divide et impera*"
Traiano Boccalini, 1556–1613

Projecting soft error rates of products is a very complex process and involves modeling at all abstraction levels, from radiation transport physics all the way up to system responses. Equations similar to (1.1) frequently form the basis of chip- or system level SER assessments. Radiation-induced upset rates of devices are modeled as the product of nominal soft error rates with timing- and architectural vulnerability factors [91, 92]. Devices in the context of Equation (1.1) are placeholder for circuits, structures, or even whole chips. Please note that the fault model assumed here is upsets occurring in memory elements (single event upsets, SEU). Upsets due to strikes in combinational logic ($\mathrm{SER_{comb}}$) are caused by so-called single event transients (SETs) and will be treated separately in Section 4.4.

$$\mathrm{SER}_{\mathrm{SEU}}^{\mathrm{system}} = \sum_{\mathrm{device}}^{\mathrm{N}} (\mathrm{SER}_{\mathrm{nominal}} \times \mathrm{TVF} \times \mathrm{AVF}) \tag{1.1}$$

Nominal soft error rates ($\mathrm{SER_{nominal}}$) refer to upset rates under static conditions, i.e., where signal propagation times are not relevant and input signals do not change. In a real chip, signals switch and propagate from device to device and not all upsets are relevant to the output of a

program. This deviation from static conditions is accounted for by two types of derating or vulnerability factors.

(A) Architectural vulnerability factors (AVF or LD: logic derating) denote the probability of faults being relevant to the execution of programs. What relevant really means in this context is discussed in Section 4.5. AVF values dependent on the application/code executed as well as the (micro-) architecture of the device. Please note that AVF in the context of Equation (1.1) is different from logic derating factors in combinational circuits (see Section 4.4).
(B) Timing vulnerability factors (TVF or TD: timing derating) equal the fraction of time during which a device is susceptible to radiation-induced upsets. TVF values depend on the device design and functionality as well as on the circuit environment (Section 4.3).

Equation (1.1) implicitly assumes that (1) the system is made up of N independent[1] devices which all must operate in order for the system to function properly (if AVF and TVF of device > 0); (2) all key variables ($\mathrm{SER}_{\mathrm{nominal}}$, AVF and TVF) are independent of each other; and (3) that the single event effect (SEE) approximation holds, i.e., that at any given point in time faults are induced by only one single ionizing particle. Multi-bit upsets (MBU), where one SEE results in the formation of more than one fault, are treated separately in Section 4.7. Device parallelism (redundancy) can be accounted for in AVF values.

Recent work by Miskov-Zivanov et al. and Rao et al. has demonstrated that for combinational and sequential logic, derating factors are not strictly independent of each other [77, 78, 108]. Re-convergent paths can break the independence of derating or masking factors in the case of SETs. Nevertheless, it is a key assumption in this work that in the case of single event upsets an independent treatment of all variables in Equation (1.1) results in accurate SER estimates for complex, general purpose chips such as central processing units (CPUs).

[1] Independent with respect to failure probabilities of the individual devices or components.

As mentioned above, Equation (1.1) is applicable to small devices/ circuits (for instance a latch) as well as to whole chips and even systems. In the former case, it equals the sum over all nodes[2] in the circuit of interest, in the latter it is the sum over all circuits or components of a chip or system. It can be easily seen that a chip- or system-level SER assessment strategy cannot possibly account for all input vectors, all circuits and signal paths. Typically, averages of TVF and AVF values over larger structures such as storage queues and execution units and over selected applications (code sequences) are simulated and applied in Equation (1.1). It is worth mentioning that if averages are applied in Equation (1.1), mitigation decisions cannot be made on a scale smaller than the averaging range. In this case the output of Equation (1.1) might be sufficiently accurate for upset rate projections, but certainly not for identifying nodes or devices as candidates for hardening.

1.2 Particle-induced Soft Error Upset Modes

Derating factors and nominal soft error rates not only depend on the technology, design and system architecture, but are also impacted by the error type. The best known and characterized single event phenomenon is the single event upset (SEU), where one single particle strike upsets a memory type cell. This could be a static random access memory (SRAM) cell, a dynamic random access memory (DRAM) cell, a latch, a register file (RF), a sense amp (SA), etc. SEU further can be classified into single bit upsets (SBU) and multiple bit or cell upsets (MBU or MCU) [56]. An MCU occurs when a single particle strike upsets several memory cells and no attention is paid to how the cells or bits are arranged logically (bytes, words, etc.). If the upset cells logically belong to the same protected entity, the phenomenon is called an MBU.

An entirely different class of upsets is formed by so-called single event transients (SETs). SETs occur in combinational logic, where the node voltage is always restored in the case of a strike. How fast depends on the charge collection dynamics,[3] the load capacitance and on the

[2] Transistors in the case of Silicon on Insulator (SOI) based circuits.
[3] Which in turn depends on the process technology and the particle strike location.

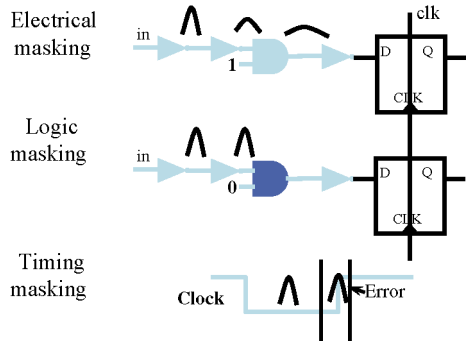

Fig. 1.1 Various masking effects of strikes in combinational logic are illustrated.

driver strength which all determine the width and amplitude of the radiation-induced voltage pulse. A fault occurs when the particle generated voltage glitch propagates to an observable output or is captured by a storage element. A radiation-induced glitch can be captured by the receiving storage element only if it is not masked by any of the following three effects (Figure 1.1):

(1) Electrical masking: pulses will be attenuated before arriving at the latching element.
(2) Logical masking: propagation of pulses is blocked by logic gates.
(3) Latching-window masking: propagated pulses will not be latched unless the pulses overlap with the setup and hold time window of the receiver.

Once an SET has been captured by a storage element (latch, FF, etc.), it becomes indistinguishable from an SEU of the receiver induced by a direct strike of one of the nodes within the device. More than one storage element can be upset by inducing an SET in combinational logic with a fanout larger than 1. See Section 4.4 for more details.

The above three masking effects depend on the electrical, logical, and timing properties of the circuit. For the pulse to propagate along the path from the struck node to the output of the combinational block, i.e., input of the storage element, the path must be logically sensitized

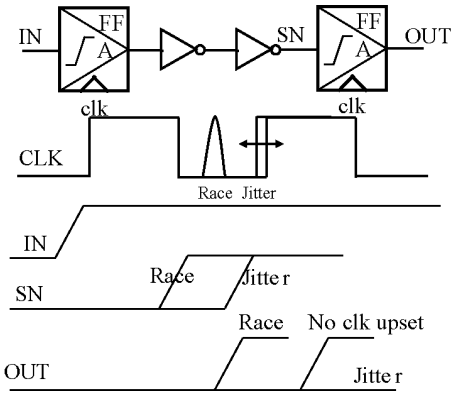

Fig. 1.2 Soft error upset modes for clock node strikes [119]. © 2005 IEEE. Reproduced with permission.

and the pulse width must be wider than the propagation delay of the slowest gate along the path [12].

Particle-induced SETs in control logic and along data paths have many commonalities with respect to SET formation and propagation. The impact on the upset rate of a circuit, however, is distinctly different. Seifert et al. investigated the impact of particle strikes in clock trees of a modern microprocessor [119]. In principle one can distinguish two modes of clock node upsets. Figure 1.2 schematically depicts both modes. IN and OUT denote the input and output nodes of one pipeline stage, CLK denotes the external clock node and SN the data path node just before the receiving sequential (an FF in this case).

(A) Radiation-induced clock jitter: clock jitter is defined as the difference in clock arrival times at one and the same clocked receiver. Charge injected into clock nodes by ionizing radiation at times that are very close to when the clock is asserted results in the clock edge moving randomly in time. In this case a setup time (T_s) violation might occur, i.e., the clock edge is shifted such that for critical paths data will not be latched correctly. Data might arrive too late at the receiving latching element (Figure 1.2 — Jitter case).

(B) Radiation-induced race: this mode reflects a false opening of a receiving storage element. For a short data path and

without any irradiative effects data would remain at the input of the receiving storage element until the clock asserts. Due to a particle strike enough charge might be injected to result in the formation of a new clock pulse. If the width of the pulse is wide enough, this could result in prematurely writing data into the receiver and incorrect data racing through the next pipeline stage. In the design community this phenomenon is called race and hence the naming convention. In Figure 1.2 the additional clock pulse results in a premature latching of the input data (see timing diagram of node OUT in the case of race). Whether this is significant depends on the path length of the next stage and whether the state racing through is different from what is currently stored in the receiver. Further, for a long data path where data arrive at the receiving sequential after the radiation-induced generation of the clock pulse, no upset occurs. This is because only the old data, i.e., data already stored in the receiver before the strike occurred, are propagating through the receiver.

Another acronym frequently used in the soft error literature is SEFI (single event functional interrupt [56]), which denotes single event upsets that cause the component to reset, lock-up, or otherwise malfunction in a detectable way. SEFI per se is not a different soft error upset mechanism, but rather a term that specifies a certain system response (see Section 1.4) to a particle induced upset that is fully captured by Equation (1.1).

All upset types discussed so far are soft in nature, i.e., the upset devices have no memory of it once the state has been rewritten.[4] In the case of single-event latchup (SEL) the lateral and vertical parasitic bipolar devices in bulk CMOS devices are turned on by the charge deposited in the Si by a particle strike [57]. Latchup short-circuits power to ground and due to the high currents involved is frequently destructive. In cases where SEL is not destructive, power needs to be recycled. SEL rates can be estimated on the chip-level using Equation (1.1) with

[4] This may, however, take longer than one cycle, since the re-written/corrected information might have to propagate to corrupted registers that are more than one clock cycle away.

an AVF of one. Please note that SEL is not possible in Si on Insulator (SOI) technologies because NMOS and PMOS devices and wells are completely insulated by the presence of the buried oxide. However, single event snapback where the lateral bipolar between drain and source is turned on by a particle strike has been observed in SOI devices [27].

1.3 The Unit of SER

Soft error rates are frequently expressed in units of FIT (failure in time), which equals 1 upset in 10^9 hours of operation. 1 FIT corresponds to a mean time between failures (MTBF) of about 114000 years.[5] For terrestrial applications, soft errors are an important reliability issue mainly for large systems consisting of hundreds or even 1000s of nodes but not for typical PCs or laptops where software bugs typically limit MTBF values [16].

1.4 System-level Error Types

Although the author of this article calls upsets in devices errors, it is important to clarify the definitions of the terms fault and error: a fault in hardware (HW) refers to an incorrect state caused by for instance a defect, or by radiation, whereas an error is the manifestation of a fault and results in a difference of computed values. A fault does not necessarily lead to an error, since it can be masked by HW or software (SW). In the remainder of this work, the author intends to stick to the above terminology only where deemed important, as in the case of AVF simulations for instance.

On the system level, soft errors can be divided up into errors that are detected but cannot be corrected (DUE: Detected Unrecoverable Errors), those that remain undetected/silent (Silent Data Corruption: SDC) and finally those that are corrected (CE, in SW or HW). Figure 1.3 illustrates the possible outcome of a single-bit upset

[5] MTBF (mean time between failures) is the expected time between two successive failures of a system and is a key reliability metric for systems that can be repaired. MTTF (mean time to failure) is typically applied to non-repairable systems and is equivalent to the mean of its failure time distribution.

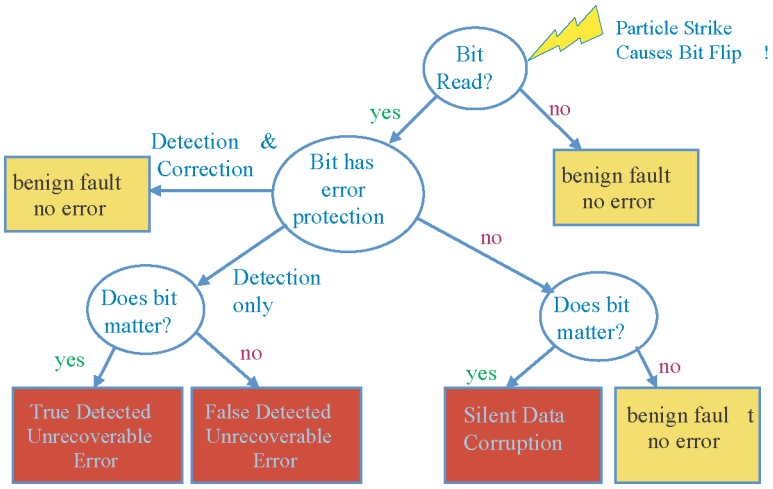

Fig. 1.3 Classification of system level soft error modes [14]. © 2005 IEEE. Reproduced with permission.

depending on whether the bit is read and on the implemented protection scheme.

From a customer's perspective silent data corruption is clearly the worst error type, mainly because the system or user is unaware of its occurrence and cannot control and prevent its propagation. Detected errors are either corrected by schemes such as error correcting codes (ECC), or re-loaded from the next memory hierarchy, or cannot be corrected (DUE) and typically result in the system rebooting. The interpretation of anomalous behavior such as a system hang is not straight forward since it is certainly detected by the user, but not through dedicated hardware level detection capabilities. The scope of DUE[6] impacts whether these error modes are factored into the DUE bucket or into the SDC one. Other authors try to circumvent this difficulty by making as many soft errors as possible detectable [49]. In this case the sum of both error types is relevant. One of the great challenges in system level radiation testing lies in making SDC detectable. In modern machine check architectures (MCA), an SDC might also trigger a detected error before the corrupted data propagate to the

[6] One example would be to account only for hardware level detection mechanisms.

program output and hence SDC is never detected. Detecting SDC in systems where DUE >> SDC is therefore very difficult. Using lock-stepped systems or some form of SW redundancy is a first step, but by no means trivial. The discussion of these issues is beyond the scope of this work.

Errors that are detected and corrected, as in the case of a single bit upset for a SECDED protected array (single error correct, double error detect), contribute to the CE rate. CE rates are of importance in lock-stepped systems for instance where the occurrence of CE can cause the system to go out of lockstep.

SEFI (Section 1.2) can be both, SDC or DUE, depending on their scopes, as long as they result in a detected (by the user or by dedicated HW) malfunction of the system.

Before modeling strategies of all key variables of Equation (1.1) are introduced, the physics of the charge collection process, the radiation environment and SER trends are discussed first.

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