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LLC Resonant Converters: An Overview of Modeling, Control and Design Methods and Challenges

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LLC Resonant Converters: An Overview of Modeling, Control and Design Methods and Challenges

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ABSTRACT

The LLC resonant converter is perhaps today's most popular resonant conversion topology. Yet, though in existence for many years, only relatively recently has it gained the popularity it certainly deserves. Since its first appearance in the literature in 1988, it has been confined for a long time to niche applications: high-voltage power supplies or high-end audio systems, to name a few.

Its significant industrial usage started in the mid-2000s with the boom of flat screen TVs, whose power supply requirements found in the LLC resonant converter their best answer, and was fueled by the introduction of new regulations, both voluntary and mandatory, concerning an efficient use of energy. This combination of events pushed power designers to find more and more efficient ac-dc conversion systems.

Since then, several other mass-produced electronic devices, such as All-In-One and small form factor PCs, high-power ac-dc adapters and LED drivers, have made a massive usage of this topology, especially in its half-bridge version. Higher power systems, such as server and telecom power supplies

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and, more recently, charging stations for electric vehicles, have mainly adopted the full-bridge version.

Over these last three decades, there has been a lot of progress on both theoretical and practical aspects related to the LLC resonant converter. Lots of papers and application notes deal with it, and many IC manufacturers have dedicated driver ICs in their portfolio. Despite that, its design is still considered a challenging task in Power Conversion. Thus, a guided tour through its intricacies may be beneficial to both the neophyte and the experienced engineer.

The monograph will cover the basics (operating modes, soft switching mechanism, first-harmonic approximation, etc.), as well as some advanced topics (design optimization, control methods, synchronous rectification, interleaving, etc.) using a hands-on, design-oriented approach.

Part I

Introduction to Resonant Conversion

1

Background

Since the beginning of the electronics era, user needs have dictated a clear trend towards size and weight reduction of electronic equipment. Of course this trend has affected power supply systems as well, as essential sub-systems for the proper operation of the equipment.

Essentially all electric equipment may benefit from size and weight reduction of their power supply. In mobile applications such as transportation, this directly translates into fuel saving or increased operating range. For portable equipment, being smaller, lighter, yet more powerful, is perceived by users as an added value. Also, stationary applications take advantage of a lower size and weight of power supplies. This makes more space available for the primary function of the installation and cuts the total cost of ownership by making installation and maintenance easier and quicker.

In power supplies, this trend is expressed by a constant demand of higher *efficiency* and *power density*, two quantities that always go hand in hand.

Efficiency is the ratio of the power output by a power supply unit (PSU) to the power that the PSU draws from the input source, being their difference (power loss) converted into heat.

Power density is a Figure of Merit (FOM) that measures the degree of compactness of a PSU. Depending on the key design goal, it can be defined in different ways, typically as the ratio of its rated power to its volume (W/cm^3) or its weight (W/kg), or scaled equivalent units. Whichever definition we consider, either volumetric or gravimetric, the power density trend can be synthesized in "packing more power in less space".

While the progress in circuit integration technology has substantially reduced the size and weight of all electronic devices, in general the miniaturization rate of power supplies has not been keeping the same pace.

Different types of power converters (ac-dc, dc-dc, point-of-load, voltage regulator modules, etc.) show different miniaturization rates. In this context we will focus on ac-dc converters, i.e., those used in power supplies operated off the ac power distribution line, the so-called *offline power supplies*.

As shown in Figure 1.1, while integrated circuit technology evolves following Moore's Law, doubling the density of transistors every approximately two years, in the last fifty years on average it takes about one decade for offline power supplies to double their power density [53]. The reasons for this slower speed will be briefly reviewed in the continuation of this discussion.

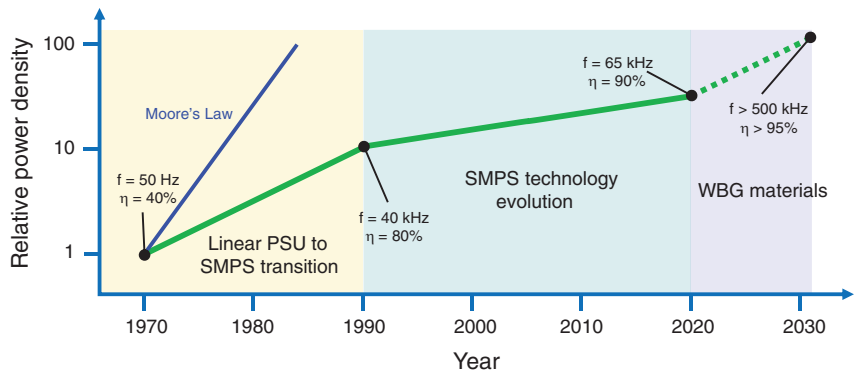


Figure 1.1: Power density trajectory in typical commercial offline power supplies.

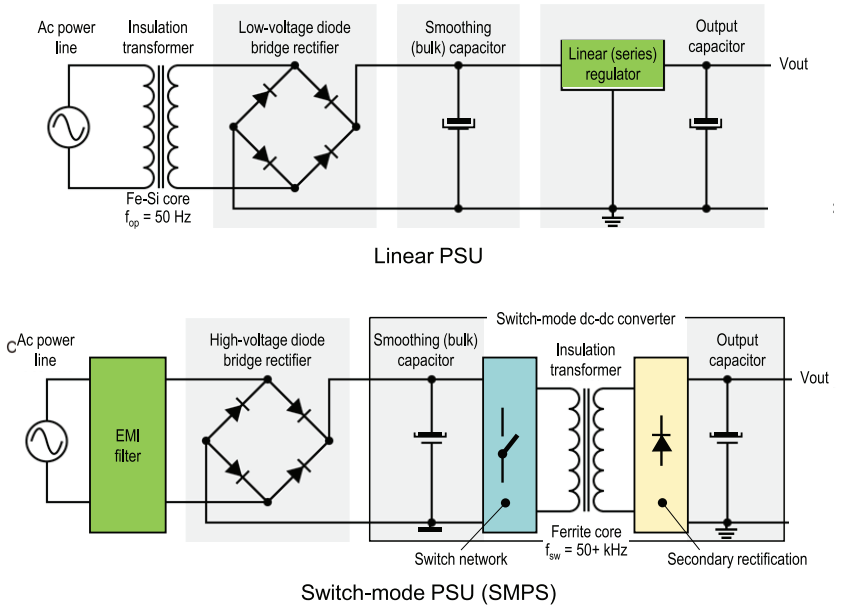


Figure 1.2: Transition from linear to switch-mode technology marked a quantum leap in size and weight reduction of offline power supplies.

This race for higher power density started with the epochal transition from linear to switch-mode power supplies, which took place at the end of the 1960s, enabled by the advent of high-voltage bipolar junction power transistors (BJT) and the development of low-loss ferrites.

Linear power supplies (see Figure 1.2) do not offer much opportunity for power density increase because size and weight are essentially dictated by the bulky line-frequency insulation transformer based on silicon iron laminations, and the heatsink. As to the heatsink, there are limited chances to reduce its size because the efficiency of linear power supplies is low and related to the input and output voltages only.

On the contrary, switch-mode technology does not need a line-frequency transformer (see Figure 1.2) and requires smaller heatsinks (or no heatsink at all in some cases) due to their higher efficiency and consequent lower amount of heat generated.

After the initial fast increase due to the linear to switch-mode transition, which represented a groundbreaking moment, in the last thirty years power density in offline power supplies has slowly increased at a rate lower than 10%/yr, despite important technology milestones such as the introduction of high-voltage power MOSFETs, which replaced BJTs, and the advancements in power magnetics.

This slower progress in power density can also be explained with a change of focus. In the early 1990s, the rapid diffusion of consumer electronics and an increased attention to environmental concerns prompted the introduction of requirements and regulations concerning light-load efficiency and standby consumption. This oriented R&D efforts towards complying with these new specifications that demanded an efficiency improvement over the entire load range and not just at full load as required by the power density targets.

Today, the tremendous growth of portable equipment has put power density again under the spotlight. With the advent of wide-bandgap materials, namely SiC and GaN, power supply industry seems to be on the verge of another fast growth period for power density, even for offline power supplies.

Why are offline power supplies (an example is shown in Figure 1.3) so difficult to miniaturize? Safety isolation (to prevent electric shock hazard), the holdup time (we need energy reservoir to keep the supplied equipment operating even during short interruptions of the ac line voltage), and the electromagnetic compatibility (EMC) requirements (not to adversely affect the operation of other electronic equipment, nor to be adversely affected by other equipment or other electric phenomena) as well as the high voltages that they are required to switch, pose quite severe obstacles in their path to miniaturization.

Though the objective is to make PSUs smaller and lighter, the ultimate technical requirement is to make them more efficient. The reason is straightforward: if we handle a given power in a smaller volume, there will be less surface area for cooling and less room for heatsinks.

It is true that this issue can also be tackled from a different angle: improving the thermal design to facilitate heat removal. However, this strategy can be pursued just to some extent. Fans can be used in some

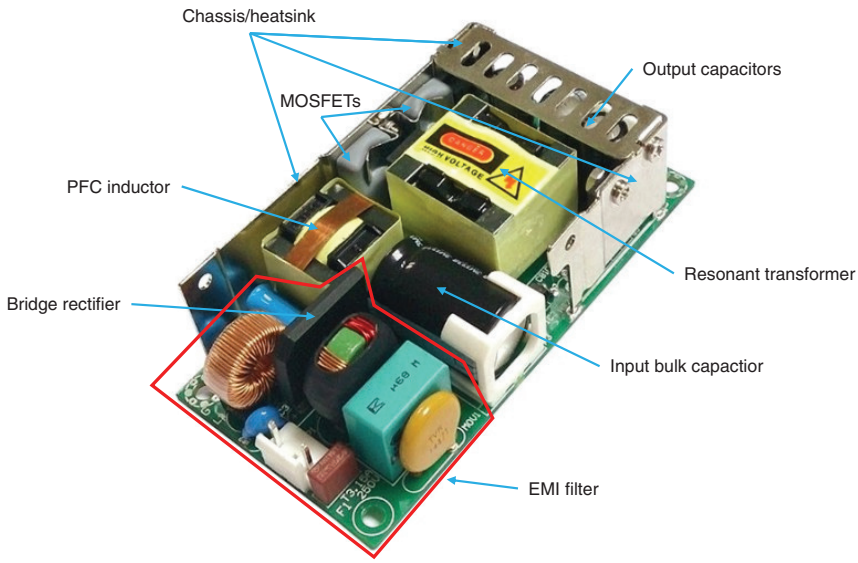


Figure 1.3: An offline power supply with its bulky parts.

applications only (e.g., telecom or server power, ATX/PS2 PC) and are out of consideration in others (e.g., ac-dc adapters and chargers for mobile equipment) for obvious reasons of user experience. Encapsulated power supplies can benefit from filler materials and other mechanical provisions that facilitate heat exchange but there are regulatory limits on the touch temperature, i.e., on the maximum surface temperature of the enclosure. In the end, if we want to increase power density we must generate as little heat as possible, which is another way to say that we need to aim at high efficiency.

Switch-mode technology is based on storing and/or transferring energy through magnetic (inductive) components, so that increasing the switching frequency brings lower inductance values and, as a general consequence, a size reduction of these devices and in some cases also of the capacitive energy reservoirs. Increasing switching frequency, therefore, is a mainstream towards smaller size PSUs. Unfortunately, this is also true only to some extent and conflicts with the requirement of high efficiency.

Switching losses and electromagnetic interference (EMI) both increase with switching frequency and any attempt to reduce switching losses by switching faster will cause more EMI that will need a bulkier filter or other provisions to be kept within the limits. Of course, slowing down switching to reduce EMI causes higher losses and impairs efficiency. This points out the need for conversion systems characterized by a low rate of rise of switching losses with frequency and, on the other hand, by a low level of EMI emissions, so that these can be kept below the regulatory limits without bulky filters (which is essential to increase power density).

Hard-switched PWM converters (intended as the classical switch-mode power processors such as buck, boost, etc. and their isolated versions flyback, forward, etc., converters that are typically controlled with a form of pulse-width modulation), can run very efficiently but not at a high switching frequency. The term "hard-switched" stems from the way switching occurs in the power devices (power switches and rectifiers) of these converters. This is commonly referred to as *hard switching* because it involves significant peaks of power dissipation due to voltage and current being simultaneously high during the transition from one state to the other. These peaks are repeated at the switching frequency, so the higher the frequency is, the larger the average power dissipation will be. These concepts will be expanded in Part II, Section 5.

A careful design and component selection may resolve part of the efficiency-EMI compromise, but simply raising the switching frequency and carefully designing the converter is not sufficient. The entire process of power conversion needs to be reconsidered for high efficiency and low EMI to increase power density via higher switching frequencies.

The reason for the keen interest that resonant converters have always attracted is that they apparently solve all the issues related to conventional hard-switched PWM converters, offering significant advantages as summarized in the following list:

- Soft switching (zero-voltage switching, ZVS, and/or zero-current switching, ZCS) significantly reduces switching losses and the energy needed to drive power switches.

- Smooth waveforms, with relatively low $\mathrm{d}v/\mathrm{d}t$ or $\mathrm{d}i/\mathrm{d}t$ stress, which relieves the strain on power components.
- Parasitic elements are part of the power processing circuit: they work *for*, not *against* the just cause of an efficient power conversion; therefore, there is no need for snubber and clamp circuits to limit unwanted and dangerous voltage and current spikes that inevitably bring additional power losses.
- Low EMI, because of both the smooth waveforms and the less noise produced by the parasitic elements; filtering requirements are less demanding.
- As a result of all the above merits, high-efficiency, high switching frequency and high power density are more easily attainable.

However, dealing with resonant converters is not exactly a bed of roses:

- Resonant converters work in a completely different manner as compared to PWM converters. They may present multiple operating modes, so they are more complicated and difficult to analyze. Both the static and the dynamic transfer functions are usually strongly nonlinear, often beyond the area of simple mathematical descriptions. This, along with the enormous diversity in the resonant converter world, may force power designers to carry out a detailed design study before selecting a topology and its modes of operation to meet a particular set of requirements.
- In most cases their nice properties are obscured by significant drawbacks (e.g., large peak voltages or rms currents, or too wide range of operating frequency).
- Resonant converters can be designed to be highly efficient in a narrow range of operating conditions. Obtaining good performance over a wide range of load currents and input voltages is difficult, in some cases practically impossible.
- Significant reactive currents may circulate in the tank circuit even when the load is removed, leading to poor part-load efficiency.

- Simulations tools (e.g., Spice, PSIM, Simetrix, ...) are helpful as a verification means but do not give much insight into overall behavior and do not provide a fast and effective way of optimization.

Additionally, there are limiting factors preventing higher frequency and power density that resonant converters attenuate just slightly or do not remove at all:

- Eddy currents in ferrite cores, skin and proximity effects in copper conductors are a major source of losses in power transformers that tend to rise significantly with the switching frequency. The smooth waveforms of resonant converters do not help much.
- For converters operated directly form the power line, resonant operation does not loosen isolation requirements nor enables any size reduction in the ac-dc front-end (input bridge plus bulk capacitor).
- Though resonant converters are more EMI-friendly, the parasitic elements in the components of the filter (essentially the equivalent series resistance, ESR, and equivalent series inductance, ESL, of capacitors, and the interwinding capacitance of inductors and chokes) tend to make the EMI filter ineffective at higher frequencies anyhow.
- The higher the switching frequency, the more the noise generated by the power switches makes the layout particularly critical to the converter's performance.
- Conduction and driving losses in switching devices. These losses cannot be eliminated but the emerging technologies of SiC and GaN switching devices, which approach ideal switches better than silicon, are making this limiting factor less and less important.

Among the crowded multitude of resonant topologies appearing in the literature and industry in the semicentennial history of resonant conversion, in the last decade one topology has emerged and conquered a dominant position: the LLC resonant converter.

Figure 1.4: Typical applications and power supplies using the LLC resonant converter.

Nowadays, this converter is at the heart of the power supply in a wide range of electronic equipment powered from the ac line (see Figure 1.4). This includes consumer applications (Desktop and AIO PCs, TVs, high-power ac-dc adapters and chargers for laptop PCs), lighting applications (street lighting and industrial lighting luminaires, high power LED drivers), telecom, server and cloud computing power, medical equipment, EV chargers and even open frame power supplies. Whenever the power level approaches hundred watts, so that it cannot be adequately served by flyback converters, or even at lower power levels when there are special requirements on efficiency or form factor constraints, the LLC resonant converter is prevalent.

At lower power levels (say, up to 500 W) the half-bridge implementation is the most common, at higher power levels designers prefer the full-bridge implementation. Of course, there is no clear boundary: it all depends on the specifications and requirements of the system as well as on cost targets.

In some cases, the LLC converter has enabled building the equipment as we see it today (for example, flat screen TVs with the internal power supply); in other cases, it has dethroned other topologies, like in the case of the desktop PC power supply, where it has almost replaced the forward converter, or the telecom power supply where it has significantly undermined the supremacy of the phase-shift full-bridge converter.

There are other resonant conversion topologies offering the favorable characteristics that we mentioned earlier, so what are the reasons for the success of the LLC converter?

In the author's view, the most sensible short answer is that the LLC resonant converter provides these benefits at the lowest level of design compromise. In other words, it offers nice properties without heavy drawbacks: it can operate both as a step-up and a step-down converter (this concept will be clarified in the following) with limited voltage stress across the semiconductor devices and an rms-to-dc ratio of primary and secondary currents only slightly larger than unity. Additionally, a wide range of output power (including no-load conditions) can be controlled with a relatively narrow variation of the operating frequency and always maintaining soft switching operation for all the semiconductor devices. To put the icing on the cake, all these benign properties can be obtained almost for free. As we will see, the LLC converter can be obtained by adding an inductor to the traditional series-resonant LC converter and this additional inductor can be realized simply by introducing an air gap in the power transformer.

With this picture in mind, it is odd that it took so long for the industry to accept and adopt it. Its first appearance in the literature dates back to 1988, whereas its massive industrial usage started in the mid-2000s. There are several reasons for that, and it is not in the scope of the present discussion to look for them. In the author's opinion, it was probably not that obvious that a significant magnetizing current in the power transformer could bring so many benefits at such low cost, hence the topology was overlooked for a long time.

To conclude this introductory picture, it is worth highlighting that the LLC resonant converter, though considered today the ultimate resonant conversion solution, still shares some unfavorable characteristics with the other resonant topologies. Complexity is one of them: there are

at least six different useful operating modes plus others that are either of no practical use or must be avoided at all. It is a strongly nonlinear system, and its dynamic properties are particularly challenging to be accurately described. After a "paper-design," a substantial simulation campaign needs to be done if one wants to really get the most out of it. However, the promises of the LLC resonant converter were so alluring that power engineers were not discouraged by that and struggled to go along its learning curve to finally dominate its intricacies.

2

Historical Outline

In 1826 the experiments of Félix Savary, a French scientist, showed the ability of an inductor-capacitor circuit to produce electrical oscillations [11]. The mathematical description of this circuit and its oscillation frequency were first determined by Lord Kelvin in 1853. In 1886 James Clerk Maxwell showed that the response of an inductor-capacitor circuit to an alternating current was at its maximum when the frequency of the alternating current and the natural oscillation frequency of the circuit were the same.

The first practical application of inductor-capacitor circuits can be found in the 1890s in the spark-gap radio transmitters, where they allowed the transmitter and receiver to be tuned to the same frequency. Heinrich Hertz, who associated the term *resonance* to the characteristics of those circuits, and Guglielmo Marconi are probably to be credited as those who most contributed to make their use in radio communications practical.

To find the first application of resonant circuits (also termed *tank circuits* or *tuned circuits*) having to do with power conversion we need to jump to 1959, when Peter Baxandall [10] invented what today is called the *class-D dc-ac resonant inverter* (or amplifier), a system capable of converting dc power into ac power and that is the basic building block of most of today's resonant converters.

IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS AND CONTROL INSTRUMENTATION VOL. IECI-17, NO. 3, MAY 1970 209

A Method of Resonant Current Pulse Modulation for Power Converters

FRANCISC C. SCHWARZ, SENIOR MEMBER, IEEE

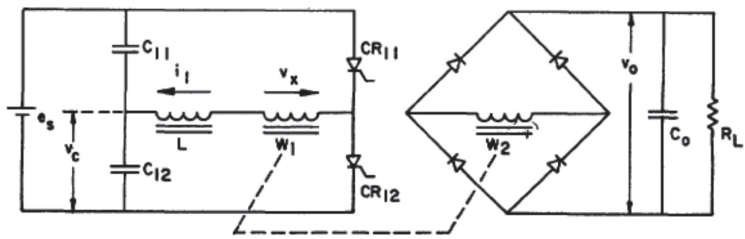


Figure 2.1: Probably the first resonant converter that appeared in the technical literature [78].

To the author's knowledge, the pioneer of resonant dc-dc power converters is Francisc Schwartz, who in 1970 published his work on a "load-insensitive series inverter-converter" [78] (Figure 2.1). With that he built a 95% efficient, 2 kW LC resonant converter operated at 10 kHz with silicon-controlled rectifiers (SCRs) as the power switches, achieving a power density of 0.4 kW/kg. This converter was intended to be used in an ion propulsion engine for spacecraft.

In a paper of 1976 [79], Schwartz improved his previous work by introducing the concept of controlling the power flow by adjustment of the phase angle between the excitation voltage and the resonant current.

The 1980s marked significant advances in the theory. Worth noting are the works from Vatché Vorpérian [87], in which he provided a complete analysis of the series and parallel LC resonant converter, those of Ramesh Oruganti and Fred Lee [66], [67] and that of Robert Steigerwald [83], which laid the foundations of the first-harmonic approximation (FHA) analysis.

In addition to the LC series resonant converter, the parallel resonant converter and the series-parallel resonant converter came onto the stage, and in a paper by Erich Schmidtner [77] (Figure 2.2) in 1988, there was

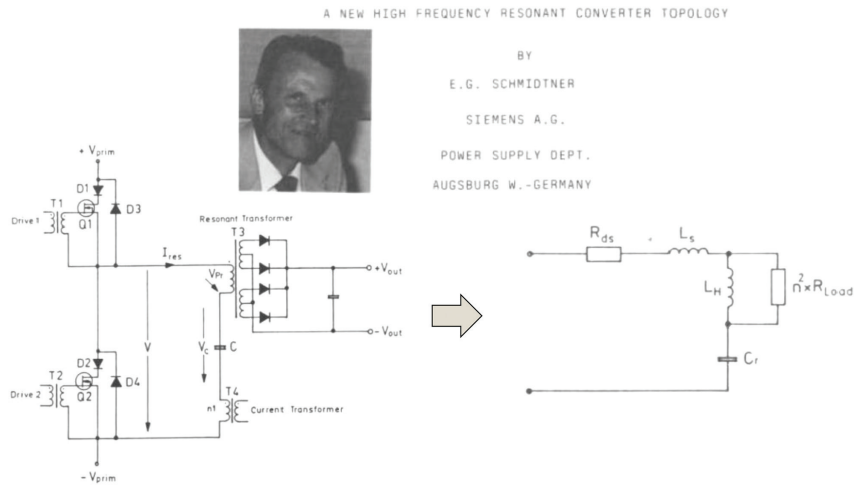


Figure 2.2: First appearance of LLC resonant converter in the technical literature [77].

the first appearance of the LLC resonant converter, though the name LLC arrived later, initially attributed to a slightly different resonant topology too.

In those years there was no noticeable industrial usage, just niche applications (e.g., high-voltage PSUs in X-ray machines), though the interest in resonant conversion in the community of power engineers was growing dramatically. In the second half of the 1980s, the first resonant control ICs appeared in the market: the LD405 and GP605 from Gennum Corp. and the CS3805 from Cherry Semiconductors were likely the first ones, soon followed by the UC3860 from Unitrode, the MC34066 from Motorola, the CS360 from Cherry Semiconductors and many others [91]. They all were low voltage ICs with ground-referenced drivers, intended to drive different types of resonant and quasi-resonant converters. To use these ICs in half-bridge topologies, gate-drive transformers were necessary to drive the high-side switch of the half-bridge leg. Noticeably, at that time high-voltage bipolar transistors (BJTs) had replaced SCRs as the power switches, and the transition from BJTs to MOSFETs had already started.

The first significant industrial usage began at the end of the 1990s and the beginning of the 2000s. Two examples: Runo Nielsen pioneered resonant power supplies in high-end audio equipment (inventing the control method [62] that today with different flavors can be found in some of the most advanced resonant controllers commercially available), and Mike Archer, one of the pioneer contributors to the development of resonant conversion technology [7], at EOS launched what was probably the first resonant ac-dc adapter for notebook PC in the market. Production volumes were not big, but resonant converters had left their niche and made their debut in the mass market.

There were two significant technology transitions and a technology development that occurred in the early 1990s that ignited the start of massive industrial usage.

The first transition was that of the electronic ballast for fluorescent lamps that was quickly replacing the old-fashioned magnetic ballast. The electronic ballast required inverters based on the half-bridge topology and initially lamp makers had no other solution than using gate-drive transformers and the associated discrete circuitry to drive the half-bridge.

The second transition concerned the power switches: the MOSFET, which appeared in the market in the 1980s, at that time was progressively replacing bipolar transistors in almost all applications due to its superior switching performance. Higher switching frequencies and power density were possible by transitioning to MOSFETs.

Realizing the big potential of these changes in the lighting market, Philips Semiconductors and STMicroelectronics jointly developed a high-voltage (600 V) Si technology, followed soon by International Rectifier. With that technology it was possible to build a high-voltage driver in a silicon chip able to drive a floating switch directly. This kit part was at the heart of the numerous high-voltage half-bridge drivers that were launched in those years and that tremendously simplified the driving circuitry of the inverter.

Soon the control functions for the lamp were integrated along with the half-bridge driver to simplify the entire BOM of the inverter. These high-voltage control ICs, which were launched in the market in the second half of the 1990s, paved the way to the high-voltage resonant

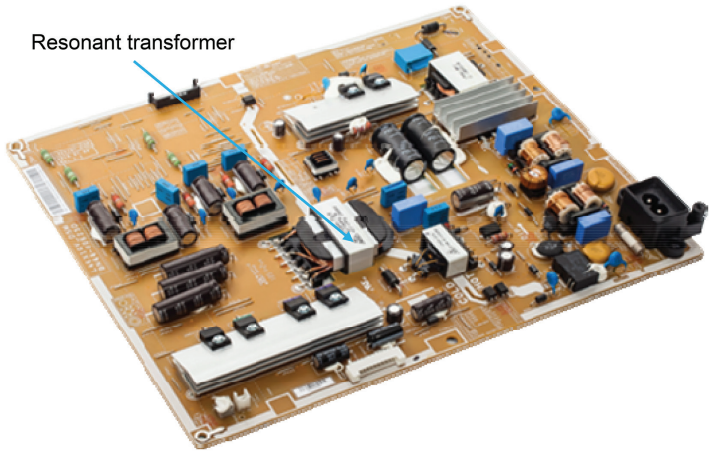


Figure 2.3: Flat screen TV SMPS using an LLC resonant converter.

controllers that were released at the end of the 1990s (ca 1998) and boomed in the next decade. The L6598 from STMicroelectronics, the TEA1610 from Philips (now NXP) and Motorola's MC33068 were probably the first high-voltage resonant controllers to be launched.

At the beginning of the 2000s there were some interesting studies that highlighted the benefits of the LLC converter over the other resonant topologies [35], [54], [92], and perhaps the growing awareness of its value triggered the real explosion of industrial usage that started amid the first and the second half of the 2000s. The killer application was the flat screen TV (LCD and Plasma at that time), where the major makers intended migrate the power supply from the external small trunk used at that time to inside the chassis (thanks also to a progressive reduction of the power demanded by the TV set). A very flat design was needed, like that shown in Figure 2.3, and the LLC converter appeared as the perfect answer and soon became dominant. Its usage was progressively extended to many other applications also supported by the proliferation of energy saving initiatives (e.g., 80+ program, EU Code of Conduct, DOE, etc.) and by market requirements getting more and more demanding. The growing industrial usage of the LLC converter, in turn, brought a proliferation of research by both industry and academia. As of today (June 2022), while another technology

transition is progressively replacing the Si-based MOSFET with the GaN HEMT (High-Electron-Mobility-Transistor), searching for "LLC converter" on IEEE Xplore provides more than 2400 results.

3

Definition and Classification of Resonant Converters

Resonant converters are switch-mode converters that include a tank circuit that actively participates in determining the input-to-output power flow. They should not be confused with quasi-resonant converters, where there is a tank circuit too, but its role is to just create the conditions for soft switching (ZVS or ZCS) with no involvement in the power transfer process.

In other words, in resonant converters the selective properties of a tank circuit (i.e., the fact that it responds primarily to stimuli having a frequency close to its resonant frequency and negligibly to other frequencies) are used to control the amplitude of currents/voltages in the converter and, ultimately, how much power transits from the input source to the output load.

As a result, resonant converters are characterized by currents or voltages that are essentially sinusoidal or piecewise sinusoidal. The low higher harmonics content of its waveforms, along with the ability of achieving soft switching for all the switching devices, explains why they are truly EMI-friendly and excellent candidates for high power density designs.

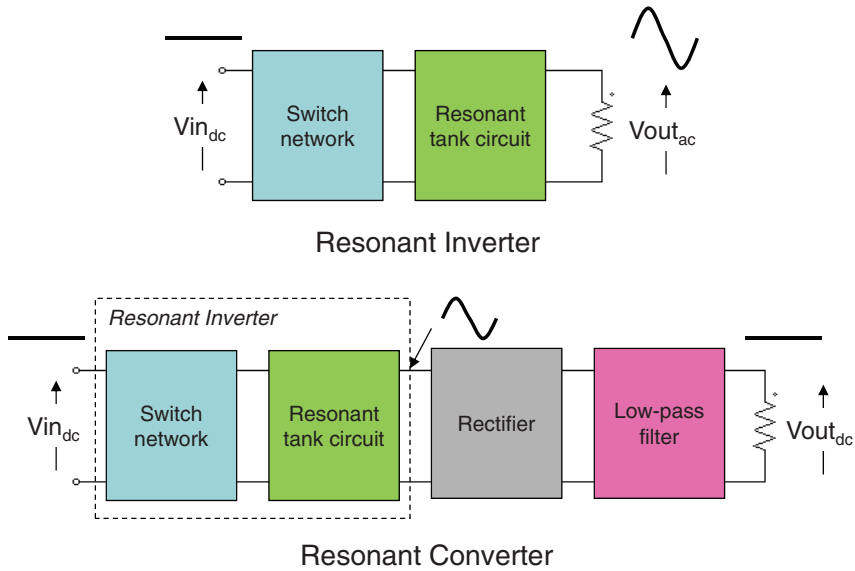


Figure 3.1: General block diagram of a resonant inverter and a resonant converter.

The family of resonant converters is an extremely broad one, and providing a comprehensive picture is not an easy task. To help get one's bearings, it is possible to consider a property shared by most of, if not all, the members of the family: they are based on a "resonant inverter", i.e., a system that converts a dc voltage into an ac voltage with low harmonic content and provides ac power to a load, with the addition of a rectifier and a low pass filter. This is illustrated in Figure 3.1.

Different types of inverters can be built, depending on the switch network and the characteristics of the tank circuit, i.e., the number of reactive elements it includes and their configuration [9]. Some assumptions will be done to restrict the analysis within the limits of the practical usage.

A fundamental one is that the switch network is connected to a voltage source and the load seen by the tank circuit can be either a voltage sink or a current sink. Additionally, the switch network drives the tank circuit symmetrically in voltage and time to produce an ac square wave voltage. Power flow will be controlled by frequency modulation,

that is, by changing the frequency of the square wave closer to or further from the tank circuit's resonant frequency.

It is worth noting that in some cases, the switch network must be coupled to the tank circuit through a dc blocking capacitor to maintain the volt-second balance across the inductive components of the tank and prevent their saturation. In other cases, one capacitor of the tank circuit may double its function as dc blocking capacitor.

These assumptions restrict the switch networks to essentially the half-bridge and the full bridge. In power amplifier terminology, switching inverters using this kind of switch network are termed *class-D resonant inverters*.

The order and the configuration of the tank circuit defines inverter's/converter's static and dynamic properties. The order of the tank circuit is the number of reactive elements it includes. It is worth mentioning that during a switching cycle, the order of the tank circuit may change under some specific operating conditions. This is commonly referred to as *multi-resonance* and, ultimately, results in a so-called *multi-resonant inverter/converter*. In case this does not happen, the converter is defined as a *single resonant inverter/converter*.

It is intuitive that the higher the order of the tank circuit is, the larger the number of possible configurations will be. However, not all these possible configurations are usable, and those that are practically used are even fewer.

With two reactive elements (2nd order tank circuits) there are eight theoretically possible configurations but only four of them are workable with a voltage source input. Two of them, shown in Figure 3.2, are commonly used: the LC series resonant tank (a) and the LC parallel resonant tank (b).

With three reactive elements (3rd order tank circuits) the number of different configurations is thirty-six, but only fifteen can be used in practice with a voltage source input. Figure 3.3 shows the two most used tank circuits: the so-called *LCC* because it uses one inductor and two capacitors with the output port in parallel to one C (a), and its dual configuration, the *LLC*, using two inductors and one capacitor, with the output port in parallel to one L.

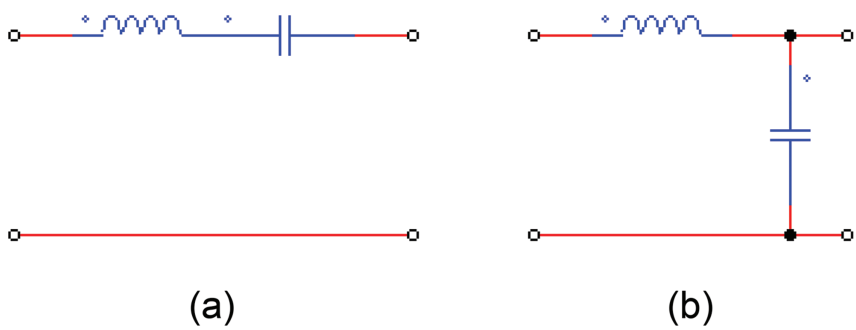


Figure 3.2: LC Series (a) and LC parallel (b) 2-element tank circuits.

The LCC tank circuit of Figure 3.3 is the core of the inverter commonly used in electronic lamp ballast for gas-discharge lamps.

With four reactive elements (4th order tank circuits) there are 182 possible configurations but those theoretically usable are less than 60. The examples of usage of 4th order tank circuits are quite rare and limited to very few of the usable configurations. Their practical meaning is, above all else, that 3rd order tanks may become 4th order when parasitic elements (junction capacitance, intrawinding capacitance, etc.) are considered. Therefore, the effect of parasitic elements on the behavior of 3rd order systems may be understood through the analysis of the 4th order system they generate.

As previously stated, for any resonant inverter there is one associated dc-dc resonant converter, obtained by rectification and filtering of the inverter output. Predictably, the above-mentioned inverters based on

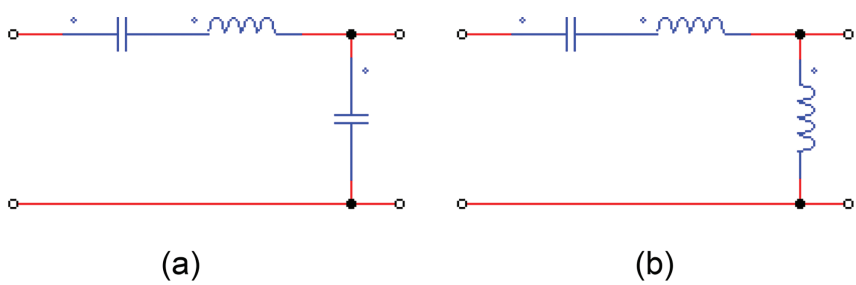


Figure 3.3: LCC (a) and LLC (b) 3-element tank circuits.

half or full bridge switch networks will originate the *class-D resonant converters*.

Considering offline applications, the rectifier block will be coupled to the resonant inverter through a transformer to guarantee the isolation required by safety regulations. The rectifier block can be configured as either a full-wave rectifier, which needs a center tap arrangement of transformer's secondary winding, or a bridge rectifier, in which case tapping is not needed. The first option is preferable with a low voltage/high current output; the second option with a high voltage/low current output. In the latter case, the rectifier block may be configured as a voltage doubler as well.

As to the low-pass filter, depending on the configuration of the tank circuit, it will be made by capacitors only (voltage sink load) or by an L-C type smoothing filter (current sink load). All these combinations of rectifier plus low-pass filter are illustrated in Figure 3.4.

Diodes are shown as rectifiers for the sake of simplicity but in real applications they are often replaced by other MOSFETs controlled to emulate the behavior of diodes (synchronous rectification). In this way conduction losses associated to rectification can be significantly reduced and efficiency increased.

Synchronous rectification (SR), which will be discussed in more detail in Part VI, Section 27, brings in several issues but also opens the door

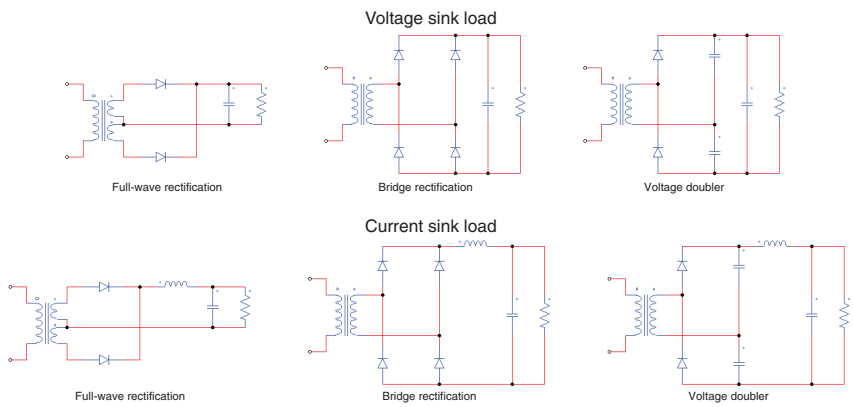


Figure 3.4: Transformer-coupled rectifier plus low-pass filter combinations.

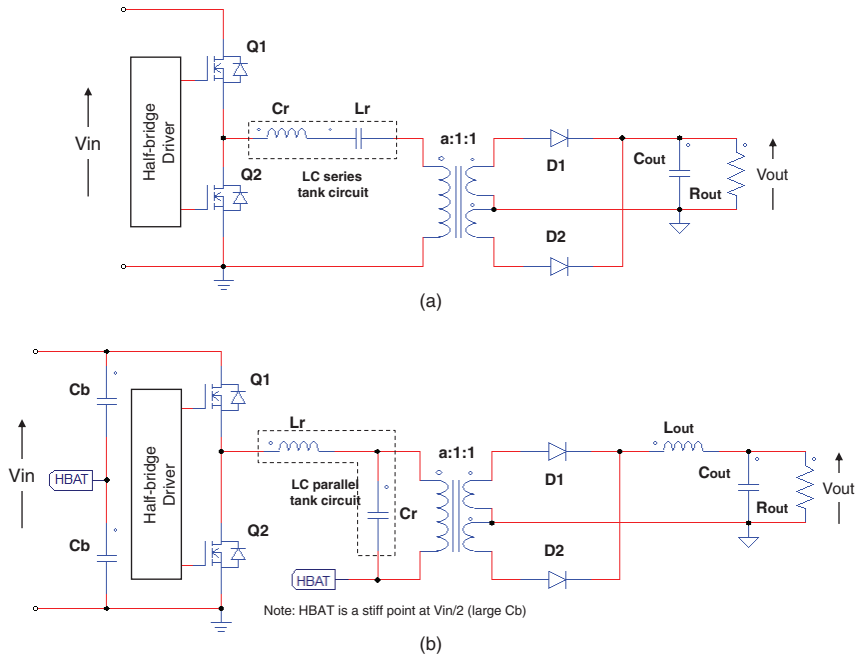


Figure 3.5: 2nd order resonant converters: (a) LC series; (b) LC parallel.

to more opportunities. With an appropriate timing of the SR MOSFET, it is possible to use phase-shift control to enhance some feature of the converter or even provide bi-directional power flow capability.

The LC series and parallel resonant tanks of Figure 3.2 are at the heart of the homonym 2nd order resonant converters, which are illustrated in Figure 3.5 in their half-bridge version and thoroughly treated in the literature [66], [67], [77], [83]. Notice that in the LC series resonant converter the resonant capacitor Cr acts also as dc blocking capacitor, whereas in the LC parallel resonant converter the two input capacitors Cb are large so that they create a stiff point (HBAT) whose voltage equals $Vin/2$. In the end, they block the dc component of the square wave generated by the half-bridge and the voltage across Cr is pure ac.

The LCC tank circuit of Figure 3.3 is the core of the homonym resonant converter when coupled to a voltage sink load [62] and of the

series-parallel resonant converter [83] when it is coupled to a current sink load. They are both illustrated in Figure 3.6. Notice that in both the series capacitor *Cs* acts also as dc blocking capacitor.

The LLC tank circuit is the core of the homonym converter that will be the subject of the following discussion.

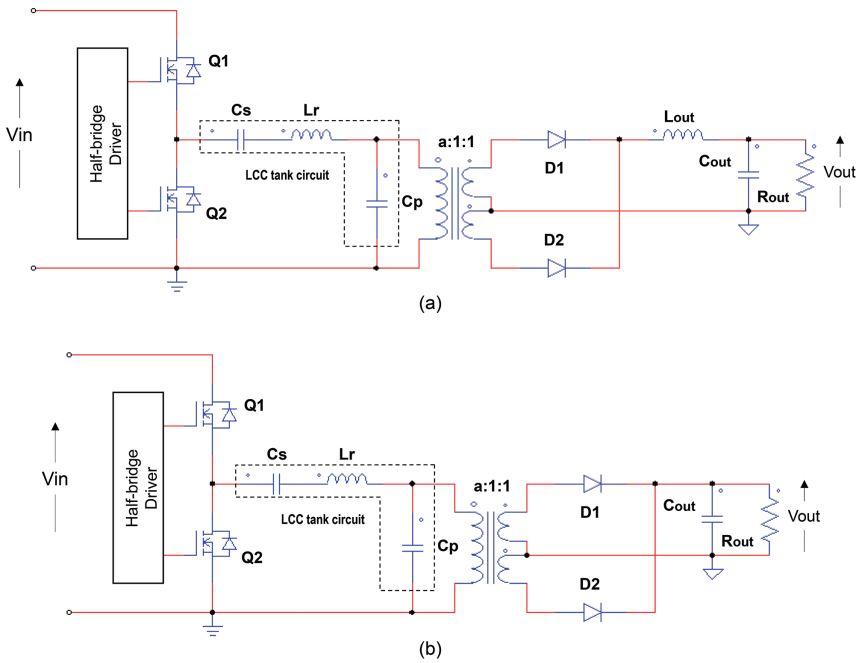


Figure 3.6: 3rd order resonant converters: (a) series-parallel converter; (b) LCC converter.

Part VI

Miscellaneous Topics

27

Synchronous Rectification

Secondary rectification losses are a major source of inefficiency in any power converter. In an LLC resonant converter that processes power very efficiently, they are very likely the top source of losses. Figure 27.1 shows the loss breakdown in a typical LLC design based on diode rectification, where the secondary conduction losses are clearly the biggest source of loss, most of them located in the diode rectifiers.

The loss of efficiency due to the secondary rectification can be easily estimated for any insulated converter. If V_{Rect} is the average forward drop across the secondary rectifiers during conduction and $Iout$ is the dc (i.e., average) output current, the power output by the transformer is $(Vout + V_{Rect}) \cdot Iout$, while that delivered to the load is $Vout \cdot Iout$. If V_{Rect} was zero all the power output by the transformer would be delivered to the load and efficiency would be unity; instead, the power $V_{Rect} \cdot Iout$ is dissipated in the rectifiers and the resulting efficiency of the rectification block is $Vout/(Vout + V_{Rect})$. Therefore the efficiency loss caused by rectification is:

$$\Delta\eta = 1 - \frac{Vout\ Iout}{(Vout + V_{Rect})\ Iout} = \frac{V_{Rect}}{Vout + V_{Rect}}, \tag{27.1}$$

which can be approximated with $V_{Rect}/Vout$ if $Vout \gg V_{Rect}$.

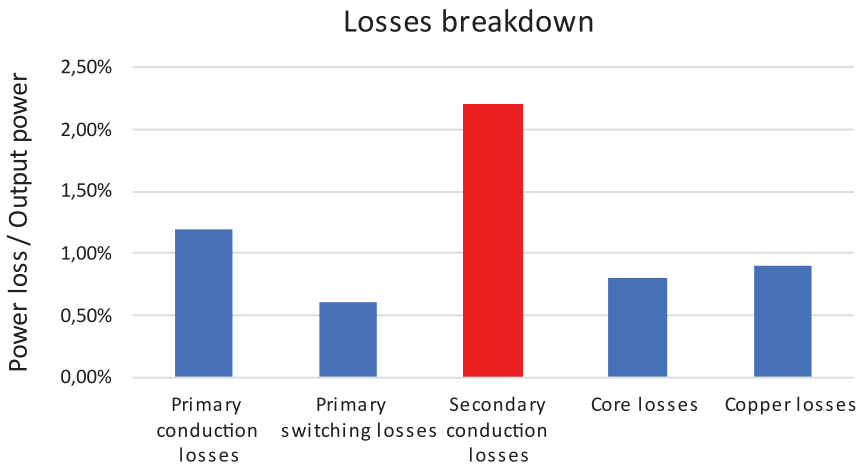


Figure 27.1: Loss breakdown in a typical LLC design with diode rectification.

With reference to the LLC converter, in the CT-FW rectification configuration it is $V_{Rect} = V_F$, in the SE-B rectification and voltage double configurations it is $V_{Rect} = 2V_F$, where V_F is the drop across a rectifier diode.

Normally, Schottky diodes are selected because of their lower forward voltage drop that, for physical limitations, cannot be reduced below approximately $0.3\,V$. Actually, Schottky rectifiers with an even lower voltage drop are available (OR-ing diodes) but their reverse leakage current is large enough to waste the benefit of a lower V_F and their use is not recommended.

To meet the demand of higher efficiency and higher power density, key to the reduction of size and weight especially in portable or handheld devices, in the late 1990s power designers began adopting Synchronous Rectification (SR), i.e., using MOSFETs in place of diodes to achieve the rectification function.

SR improves efficiency, reduces thermal performance requirements allowing higher power density, increasing reliability and decreasing the Total Cost of Ownership (TCO) of power supply systems.

In fact, the on resistance, $R_{DS}(on)$, of MOSFETs can be lowered, either by increasing the die size or by paralleling multiple discrete devices to the point that the resulting V_{Rect} of MOSFETs can be significantly

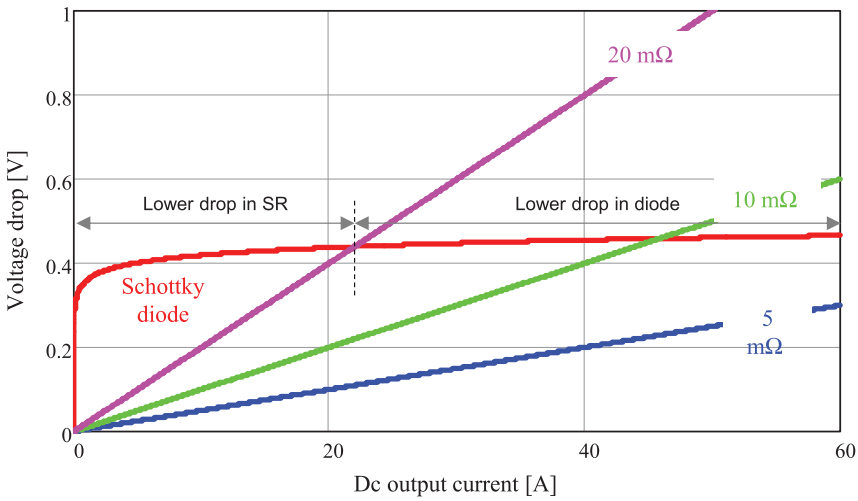


Figure 27.2: Voltage drop of a 60 A Schottky diode vs. SR MOSFET with various $R_{DS}(on)$.

smaller than the V_F of a properly sized diode at a given current. This is shown in Figure 27.2. Figure 27.3 shows the comparison of power losses. Diode losses are almost linear with the load, whereas MOSFET losses are parabolic, therefore at a current high enough diode losses can be lower, as shown in the plot on the left-hand side. Notice that the load level where SR losses equal diode losses is lower than that where voltage drops are equal: losses in diode depend on both the dc level and the rms level, those in SR MOSFETs depend on rms only.

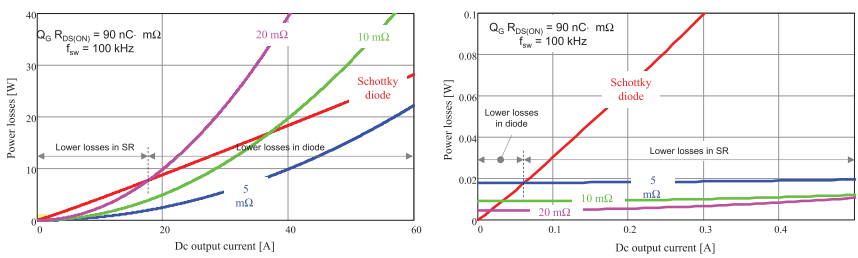


Figure 27.3: Power losses in a 60 A Schottky diode vs. SR MOSFET with various $R_{DS(on)}$: full range (left), zoom at low current range (right).

The use of MOSFETs brings additional losses due to the energy needed to drive their gate, however on the one hand MOSFETs generally work with soft-switching so that they require less gate charge Q_G and driving energy, on the other hand, MOSFET manufacturers have constantly introduced new technologies featuring lower $R_{DS(on)}$ and total gate charge Q_G, which have made SR more and more advantageous. As shown in Figure 27.3 on the right-hand side, these driving losses are anyway a loss pedestal that at very low current make total SR losses higher than those in the diode. This suggests that at a very light load it might be advantageous not to drive any more an SR MOSFET and let their body diode conduct.

Just to give a quantitative idea of a typical efficiency gain that SR can provide, it is useful to refer to Table 27.1, which shows the comparison of the efficiency of the same unit, the 240 W LLC converter specified in Table 22.2, with diode rectification and SR.

At full load there is an increase of 2.74% that becomes +2.42% at 50% load. It is worth noting that a reduction of the power dissipated in the secondary rectifiers means a lower power processed by the transformer that, in turn, causes a slight reduction of the losses on the primary side.

The use of MOSFETs, in addition to the previously mentioned benefits, also brings some issues. Of course, the need for controlling the SR MOSFETS increases the circuital complexity, but this is amply compensated by the benefits. The biggest issue in SR is that it creates for the secondary current the possibility to reverse in case of improper driving, which is something that does not happen with diodes. Since

Table 27.1: Efficiency comparison @ $Vin = 400V$ for the 240 W PSU specified in Table 22.2.

	Vout **[V]**	***Iout*** [A]	***Pout*** **[W]**	***Pin*** **[W]**	η **(%)**
SR MOSFET					
(2.5 mΩ, 40 V)	11.98	19.23	230.37	242.50	95.00
	11.99	10.00	119.90	127.10	94.33
Schottky diode					
(2 // 20 A, 40 V)	11.98	19.23	230.37	249.70	92.26
	11.99	10.00	119.90	130.45	91.91

MOSFETs are bidirectional devices, if they are erroneously turned on in a time interval when a diode in their place would be reverse biased, the secondary current will reverse.

A significant reversal may disrupt converter's operation and lead to catastrophic failures but even a modest reverse current can be a source of troubles because a SR MOSFET turned off with a reverse current will be subject to large voltage spikes that may exceed its rating. In the end, current reversal is the number one enemy of SR and must be prevented at all costs.

Essentially all topologies, both non-isolated and isolated, can be synchronously rectified. In isolated topologies providing adequate gate drive signals with the right timing to the SRs, to make them emulate the behavior of a diode is more challenging.

As illustrated in Figure 27.4, there are two fundamental types of driving techniques for SR MOSFETs of isolated topologies: self-driven and primary-control-driven SR.

The primary-control-driven method utilizes the PWM signal generated on the primary side to derive the gate drive signal for the SR MOSFET. This method requires an extra isolation circuit to transfer the timing signal or the gate drive directly to the secondary side

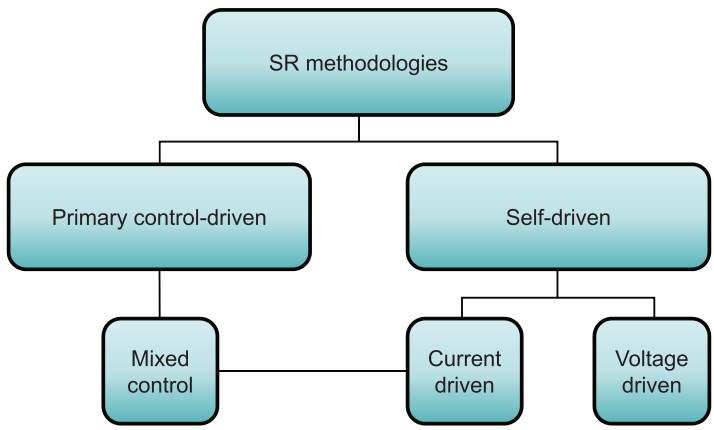


Figure 27.4: SR driving methods for isolated topologies: classification.

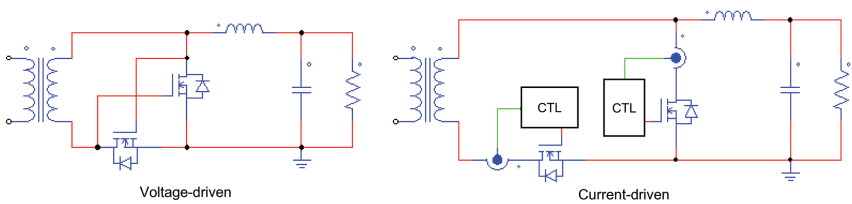


Figure 27.5: SR self-driving methods for isolated topologies: voltage-driven and current-driven.

and is applicable when the conduction timing of the secondary side is synchronized to the on and off timing of the primary side.

As regards LLC converters, this match in timing occurs only in a CCM mode operation. In case of a DCM mode, since MOSFETs conduct in both directions, the secondary current will reverse during the time interval where it is supposed to be zero. This method, therefore, is not recommended for LLC converters.

Self-driven SR can be done in two ways: voltage-driven and current-driven. Their basic principle is shown in Figure 27.5 considering the example of a forward converter.

In the voltage-driven method, the gate drive signals are taken from the secondary winding directly or from an auxiliary winding of the transformer, with just few external discrete parts or none at all in some fortunate cases.

The method is simple and low cost but is suitable for voltage-fed topologies with an inductive output filter, where the changes in the polarity of the secondary winding voltage are driven by the primary side. Besides, it works well when the secondary winding voltage is a square wave.

Coming to resonant converters, this method could be applicable to the LC parallel resonant converter (see Figure 3.5(b)) or the series-parallel resonant converter (see Figure 3.5(a)). However, the sinusoidal shape of the secondary voltage waveform makes the driving voltage low at the beginning and the end of the conduction interval, causing higher conduction losses.

The voltage-driven method is not applicable to the LLC converter, which is a current-fed capacitor-loaded topology, where the polarity of

the voltage on the secondary winding can change only after the SR MOSFET is turned off (as long as current is flowing on the secondary side, the voltage on the secondary winding is fixed at *Vout*).

With the current-driven method the current flowing through the SR MOSFET is sensed and the information is processed by a control circuit to turn it on or off properly. The good point is that this method is applicable to any topology because a current-driven SR MOSFET can in principle really emulate a diode.

Sometimes it is possible to find SR control solutions that are a combination of the primary-control-driven method and the self-driving current-driven method. In this case, the information from the primary side is typically used to turn on the SR MOSFET and the current information to turn it off. This methodology combines also the complexity of the two approaches, so it is typically used when the conditions are such that a full self-driving current-driven method does not ensure reliable operation.

From now on the discussion will focus on the self-driving current-driven method. The approach is apparently straightforward and perfectly matching the characteristics of the secondary currents in the LLC converter, which start from zero and go back to zero at the end of the conduction period. We will see that, instead, it poses challenges that are not easy to tackle.

The most appropriate way to sense the SR MOSFET current is by using a current transformer, but in an LLC converter we need two of them, which has a not negligible impact on PCB real-estate, power losses and cost. For this reason, using the $R_{DS(on)}$ of the SR MOSFET in the on state as a sense resistor has become an industry standard current sensing method for SR control, available in many commercial ICs (and not only for LLC converters).

This solution is successful despite its accuracy and reliability being highly affected by several adverse factors. It is not only the tolerance and the temperature dependence of the $R_{DS(on)}$ of the SR MOSFET that come into play but also its package and the layout of the printed circuit board (PCB). Last but not least, the fact that the control operates on signals in the mV range that live together with gate driving

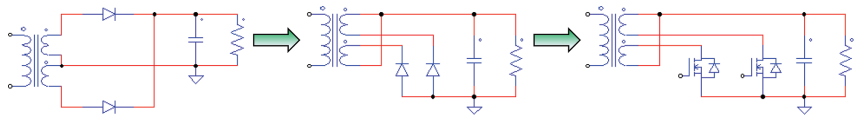


Figure 27.6: Rectifier relocation in CT-FW configuration for ground-referenced driving.

pulsed currents and secondary currents of several amperes makes its implementation in a control IC all but simple.

SR Configurations in LLC Converters

As seen in Part II, Section 4, the rectifier block in LLC converters can be configured as either a full-wave rectifier, which needs a center tap arrangement of transformer's secondary winding (CT-FW configuration) or as a bridge rectifier, in which case tapping is not needed (SE-B configuration). It is worth reminding that the first option is preferable with a low voltage/high current output and the second option with a high voltage/low current output. In the latter case the rectifier block may be configured also as a voltage doubler (VD configuration).

In case of CT-FW configuration, replacing diodes with MOSFETs needs a preliminary relocation of the rectifiers so that they can be driven ground-referenced. The steps of this modification are shown in Figure 27.6. Each rectifier is moved to the other side of each half-winding so that their anode is connected to ground, then they can be replaced by source-grounded SR MOSFETs that can be easily driven. Notice that the SR MOSFETs will normally work in the third quadrant, i.e., current will flow from the source to the drain.

In case of SE-B rectification, replacing all diodes with MOSFETs necessarily involves SR MOSFETs that need a floating driver. Sometimes an acceptable cost-performance tradeoff is represented by the so-called semi-active bridge, where only the two low-side diodes of the bridge are replaced by MOSFETs. Both solutions are shown in Figure 27.7.

Of course, it is possible to synchronously rectify also the voltage doubler configuration, which essentially requires a half bridge leg. However, normally the voltage doubler configuration is used when the output

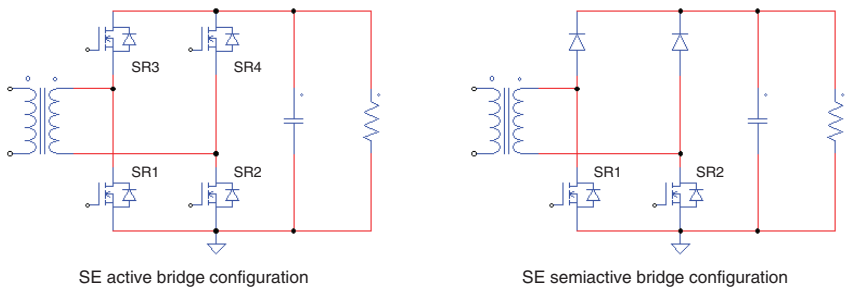


Figure 27.7: Synchronous SE-B rectifier configurations.

voltage is very high, where synchronous rectification offers quite limited benefits, so it will not be taken into consideration.

Normally in the SE-B rectification the driving scheme of the four SR MOSFETs aims to emulate the behavior of the diode bridge, where the two diagonals conduct alternately: SR1 and SR4 are driven on and off simultaneously, like SR2 and SR3 but with opposite phase. In this case the control action can be exercised on the low-side MOSFETs only and the control requirements and solutions are not different from those of the CT-FW configuration.

With different driving schemes, where for example there are time intervals where SR1 and SR2 (SR3 and SR4) are both in the on state, or by properly shifting the driving signals of the primary side switches in a full bridge with respect to those of the SR MOFETs, it is possible to enhance some feature of the converter or even provide bi-directional power flow capability. These aspects are beyond the scope of the present discussion and will not be considered.

In the end, we will concentrate the following discussion on the CT-FW configuration where the SR MOSFET are controlled with the self-driving current-driven method, and with the implicit assumption that all that will be said can be extended to the case of SE-B configuration as well.

The system we will refer to is illustrated in Figure 27.8. Its operation can be simply described as composed by three phases that are equal for both secondary half windings:

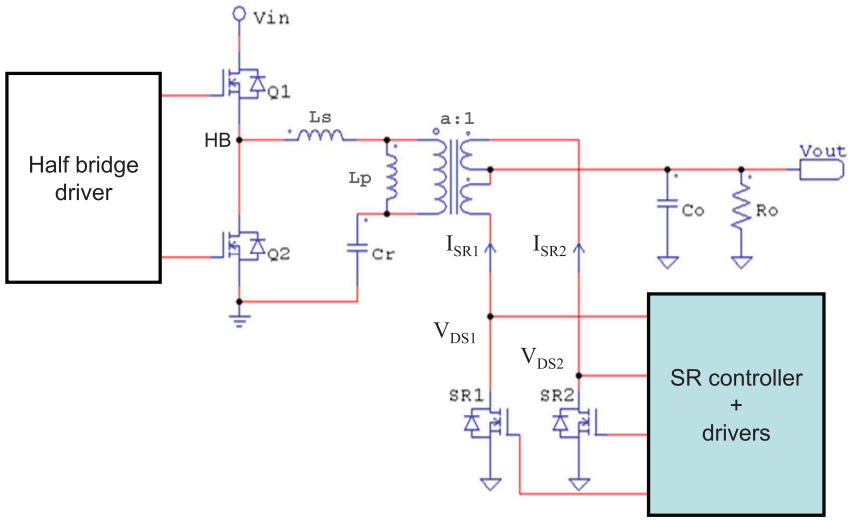


Figure 27.8: Synchronous CT-FW configuration (reference).

(1) The secondary current through either half winding (I_{S1} or I_{S2}) starts flowing into the corresponding SR MOSFET body diode.

(2) The SR controller detects the diode conduction (drain-source voltage becomes slightly negative) and switches on the SR MOSFET; notice: this is a ZVS turn-on anyhow.

(3) The SR controller detects that the current of the SR MOSFET in the on state is zeroing and switches it off.

To implement this ideal behavior, illustrated in Figure 27.9, the SR controller will be provided with at least a pair of comparators. The first one will be referred to a slightly negative voltage V_{TH_ON} and responsive to a negative-going edge of the drain voltage V_{DS} to detect the onset of the body diode conduction and drive the SR MOSFET on. The second comparator (Zero-current comparator, ZCC) will be referred to a negative voltage V_{TH_OFF} very close to zero and responsive to a positive-going edge of the drain voltage V_{DS} to detect the zeroing of the current in the SR MOSFET and whose output is used to switch it off.

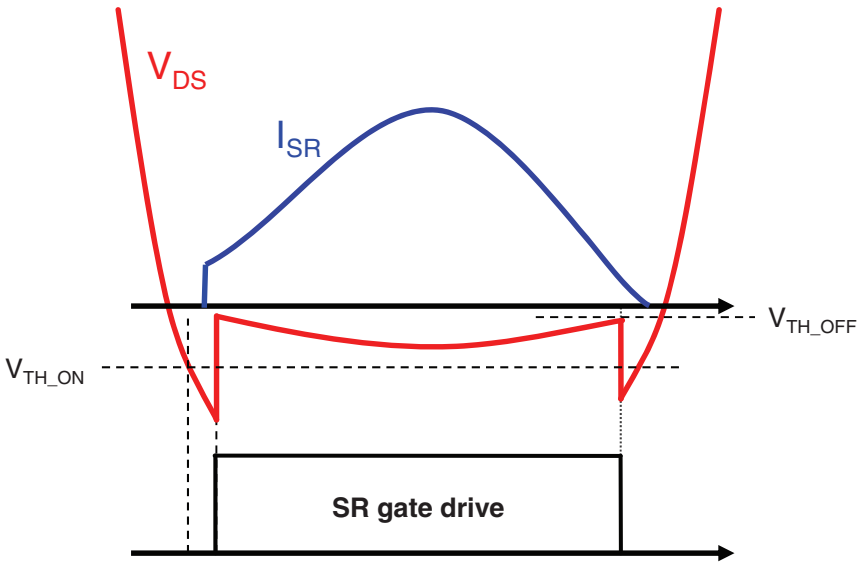


Figure 27.9: Ideal behavior of a SR MOSFET in LLC converters.

Before examining in detail the challenges posed by the SR control, it is convenient to re-examine the shapes of the secondary currents under the various operating conditions that have been described in Part III, Section 10.

Figure 27.10 shows the typical secondary current in a half winding and the cathode-to ground voltage across the rectifier (a diode), along with the gate drive waveform that the SR controller should generate.

At turn-on, the secondary current shows a step-change that is smaller at resonance and below resonance, and a bit larger above resonance. This is due to the parasitic capacitance of the secondary rectifiers, which has been discussed in Part III, Section 10 and Part IV, Section 17 dealing with the feedback reversal phenomenon. This initial current causes the secondary rectifiers to lose exact ZCS at turn-on, but as long as the secondary current is large enough this initial current is embedded in the current generated by the normal energy transfer mechanism and does not pose any special problem to the SR control.

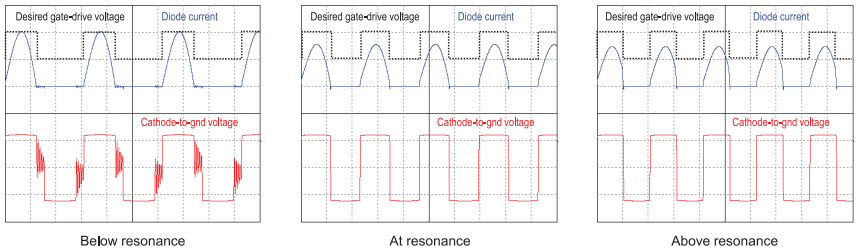


Figure 27.10: Secondary-side current and voltage at full load in a half-winding of CT-FW.

However, at light and very light load the superposition of the two contributions can even split, originating two distinct conduction intervals, as depicted in Figure 27.11 that shows the same waveforms as in Figure 27.10 with a progressively lower load from left to right.

ZCS at turn off is confirmed under all conditions. The most critical situation for the zero-current detection to turn off the SR MOSFET is above resonance, where the last portion has a very large $\mathrm{d}i/\mathrm{d}t$ thus requiring ultra-fast detection and turn-off.

SR Control Challenges: SR MOSFET Turn-On

Let us assume that the converter is operating at a load not too light, such that the waveform of the secondary current is like one of those shown in Figure 27.10 or like the first two scope pictures from the left of Figure 27.11.

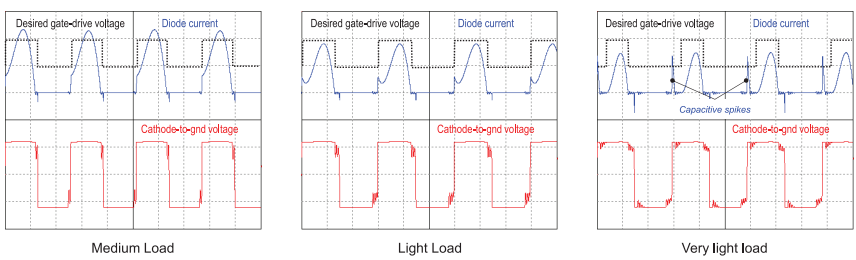


Figure 27.11: Secondary-side current and voltage vs. load in a half-winding of CT-FW.

As mentioned earlier, the SR MOSFET should be turned on when V_{DS} becomes more negative than V_{TH_ON}, a slightly negative threshold (e.g., $-0.3V$), which denotes that body diode is about to conduct. However, as the SR MOSFET is turned on, its V_{DS} collapses from the drop $-V_F$ of forward biased diode to a very low value ($V_{DS(on)} = -I_{SR} \cdot R_{DS(on)}$) and this could be erroneously taken for current zeroing should this voltage exceed the turn-off threshold. This is quite likely because I_{SR} is initially small, thus the SR MOSFET could be prematurely turned off.

To prevent this erroneous behavior the SR controller typically provides a blanking time during which the ZCC output is ignored, to let $I_{SR}(t)$ build up below the zero current detection threshold. This is illustrated in the time diagram of Figure 27.12.

This blanking time is useful to filter the noise generated by the SR MOSFET turn-on too. This noise can be anyway minimized by using a gate driver with a low source current capability: in fact, the SR MOSFET is turned on with ZVS so there is no need to turn it on fast.

The blanking time determines a minimum on-time for the SR MOSFET, thus its duration will be a tradeoff between preventing the SR

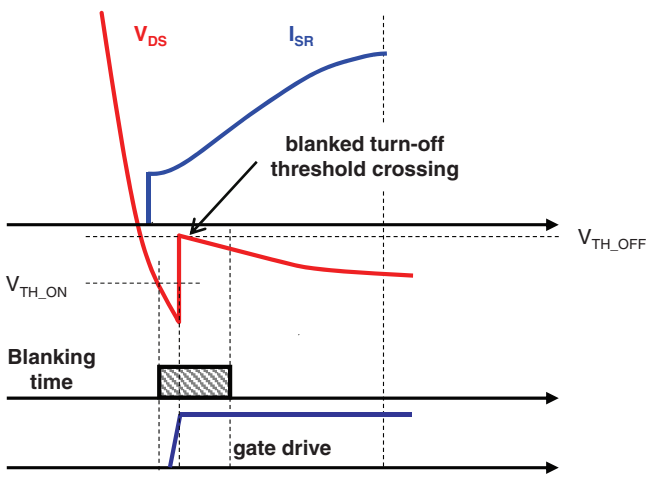


Figure 27.12: SR controller operation at turn-on of SR MOSFET: turn-off blanking time.

MOSFET from misbehaving during normal operation and the need of turning it off as quickly as possible in case of an abnormal operating condition that causes the secondary current to reverse just after the beginning of the conduction period.

As visible in the rightmost oscillogram of Figure 27.11, when the load is very light the initial non-conductive period of the DCMAB mode lasts longer than the duration of the initial current injection so that there are two distinct conduction intervals in a half-cycle. The initial spike also has an amplitude comparable to that of the "main" conduction.

The initial current may prematurely turn-on the SR MOSFET, i.e., when the secondary voltage is not yet large enough to make it work in the third quadrant, as shown in the timing diagram of Figure 27.13. Therefore, as the capacitive injection ends, the secondary current will reverse until the secondary voltage builds up to the point that the main conduction starts. This current reversal discharges the output capacitor acting as a sort of *dummy load*, which increases the rms current, lowers efficiency, and may induce the converter to oscillate.

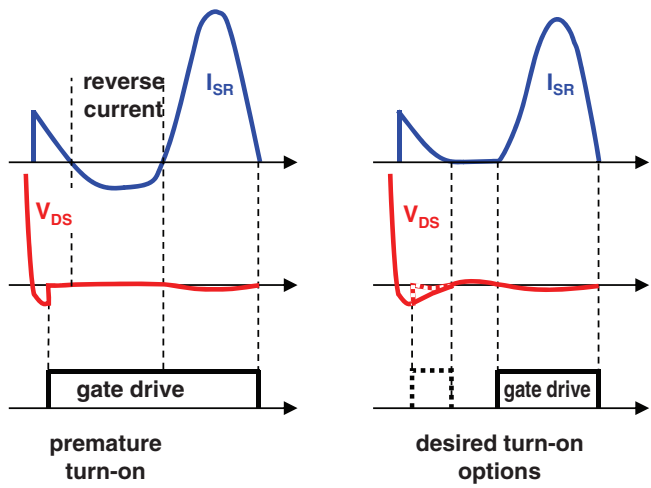


Figure 27.13: SR controller behavior at turn-on of SR MOSFET with a very light load.

Ideally, either the turn-on should be delayed until the main conduction takes place or accept a dual turn-on/turn-off in a switching half-cycle. The first solution costs some power loss due to the flow of the initial current through the body diode, then with a much larger voltage drop, the second implies a waste of driving energy. Both solutions adversely affect the input power consumption and the better option depends on the specific design.

An elegant implementation of the first solution is an adaptive control that automatically synchronizes the turn-on instant to the main conduction interval under essentially all operating conditions. Its operation can be described with the aid of Figure 27.14 and includes the following steps that are equal for both secondary half windings:

(1) When the drain-source voltage V_{DS} falls below the turn-on threshold V_{TH_ON} the SR MOSFET is turned on after a certain delay T_{D_On}. This delay is initially set at a certain point of the adjustment range, which is normally proportional to the duration of a switching half-cycle.

(2) After a blanking time T_{BLK} following turn-on (to prevent a premature turn-off), if current reversal is detected (ZCD event), the delay T_{D_On} is increased in the next conduction half cycle, otherwise it is unchanged.

(3) If no current reversal occurs in a given number of consecutive switching cycles, the delay T_{D_On} is decreased in the next conduction half cycle to check if conditions have changed and a shorter T_{D_On} is sufficient to prevent current reversal.

This functionality, with slight variations, can be found in several commercial ICs.

SR Control Challenges: SR MOSFET Turn-Off

Despite the secondary rectifiers always turn off with ZCS, generating the proper timing of SR MOSFET turn-off is far from being trivial, rather it is probably the most challenging aspect of SR control.

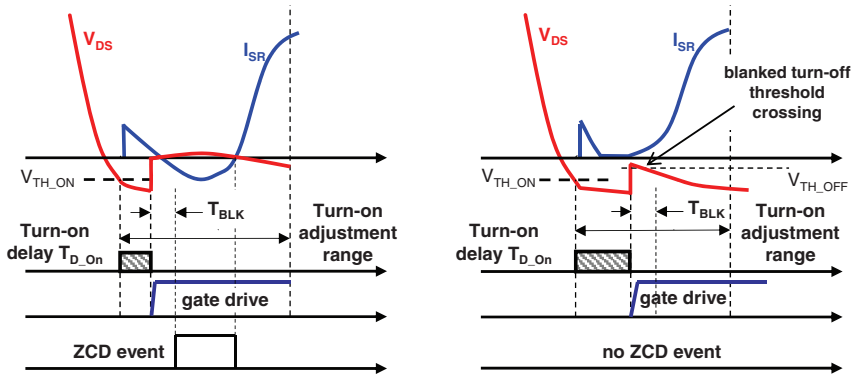


Figure 27.14: Principle of adaptive turn-on delay.

On the one hand, the SR MOSFET must be turned off before the secondary current reverses to prevent all the troubles that even a slight current reversal causes. On the other hand, if the SR MOSFET is turned off too early, current will go on flowing through the body diode, then with a much higher voltage drop and, consequently, much higher power. This will significantly hurt efficiency, so the residual conduction time, if any, should be as short as possible.

Fulfilling both requirements under all static and dynamic operating conditions is the challenge, which is made sharper by the non-monotonic shape of the secondary current waveform.

As previously said, in principle the matter is quite simple: since we are sensing the drain source voltage, $V_{DS(on)} = -I_{SR} \cdot R_{DS(on)}$, a comparator referred to a negative voltage very close to zero and responsive to a positive-going edge of the drain voltage (ZCC) will serve the purpose of detecting the zeroing of the current. However, there are several issues that need to be addressed.

A first issue is represented by the accuracy of the turn-off threshold V_{TH_OFF}: its value is in the mV, the same order of magnitude as the input offset voltage of a real-world comparator, which can therefore be the biggest source of inaccuracy. The input offset can be reduced by making the input differential pair physically bigger but this slows down the response of the ZCC, and here we need to be very fast in detecting the zero-current condition and turning off the SR MOSFET (typically

less than 30 ns). Techniques such as chopper amplifiers, autozeroing or other offset cancellation techniques can be utilized to reduce the input offset to levels that have a minor impact on the threshold accuracy.

A second issue is the ZCC propagation delay and its dispersion, i.e., its dependence on temperature, slope of the input signal and overdrive (no common-mode dependence in this case, since the comparator is essentially referred to zero). Special circuital configurations and design techniques are necessary to achieve a very fast comparator with low propagation delay dispersion because the ZCC is required to work with a very small input signal, then with a very small slope, and tiny overdrive.

As to the gate driver, whereas a low source capability is required to turn the SR MOSFET on, a much larger sink capability (several Amps) is needed to turn the SR MOSFET off as quickly as possible. Additionally, also its propagation delay must be very short (in the 10 ns) because it adds up to the propagation delay of the ZCC to determine the overall turn-off delay of the SR controller.

In addition to these implementation issues, there are a couple of system-level issues that need to be taken into consideration.

A first system-level issue can be easily solved: realistically, the SR MOSFET will be turned off slightly before its current zeroes, to have some safety margin against current reversal. Therefore, its V_{DS} will suddenly go from nearly zero to $-V_F$ to let the residual current flow through the body diode of the SR MOSFET until it actually zeroes. The turn-on threshold V_{TH_ON} will be definitely crossed but this must not cause the SR MOSFET to turn on again. Typically, either a blanking time after turn-off or an appropriate control logic can prevent an erroneous turn-on.

A second issue, the so-called *inductive early turn-off* illustrated in Figure 27.15 along with its root cause, is much more difficult to solve and has been the topic of extensive research over the last fifteen years [20], [21], [27], [29], [31], [32], [34], [47], [89].

The intent of measuring the drop across the SR MOSFET $R_{DS(on)}$ is deceived by the packaging of the SR. The stray inductance of the package (and the PCB traces if the layout is not well optimized), makes the sensed drain-source voltage V_{DS} differ from the drop V_{ON} across

$R_{DS(on)}$:

$$V_{DS}(t) = R_{DS(on)} I_{SR}(t) + L_{stray} \frac{dI_{SR}(t)}{dt}, \tag{27.2}$$

where $L_{stray} = L_{source} + L_{drain} + L_{trace}$. Therefore, in the final part of the half-cycle, where $\mathrm{d}I_{SR}(t)/\mathrm{d}t$ is negative, the drop on L_{stray} is negative and the sensed voltage V_{DS} is smaller than V_{ON}. As a result, V_{DS} will cross the turn-off threshold V_{TH_OFF} well before V_{ON} would do, causing the SR MOSFET to turn off when I_{SR} is still well above zero. I_{SR} will go on flowing through the body diode until zeroing, but the higher voltage drop will significantly hurt efficiency.

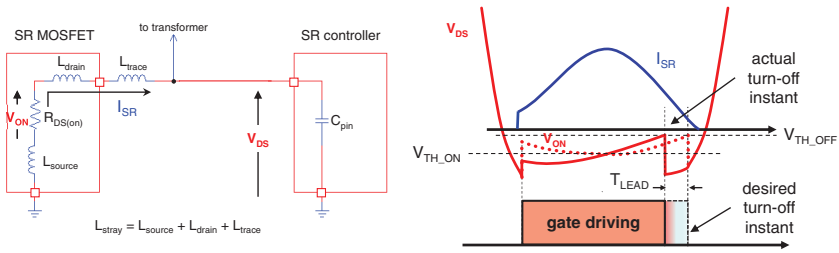


Figure 27.15: Inductive early turn-off: root cause (left), key waveforms (right).

Considering that V_{TH_OFF} is so small that it can be considered zero, the leading time T_{LEAD} shown in Figure 27.15 i.e., how much earlier the SR MOSFET turns off with respect to the actual zero of the secondary current, can be estimated with the following formula:

$$T_{LEAD} = \frac{1}{2\pi f_{sw}} \tan^{-1}\left(2\pi f_{sw} \frac{L_{stray}}{R_{DS(on)}}\right). \tag{27.3}$$

L_{stray} and $R_{DS(on)}$ are the parameters of a lossy inductor representing the SR MOSFET in the on-state and the argument of the tan^{-1} function can be regarded as the quality factor Q of this inductor.

The plot on the left-hand side of Figure 27.16 shows the plot of the normalized T_{LEAD} ($2T_{LEAD} \cdot f_{sw}$) given by (21.46) as a function of f_{sw} for different values of the ratio $L_{stray}/R_{DS(on)}$, where $R_{DS(on)}$ is fixed at 10 mΩ and the typical value associated to various packages is used for L_{stray}; the plot on the right-hand side of Figure 27.16 shows the plot of the normalized T_{LEAD} as a function of the quality factor Q of the lossy inductor representing the SR MOSFET in the on-state.

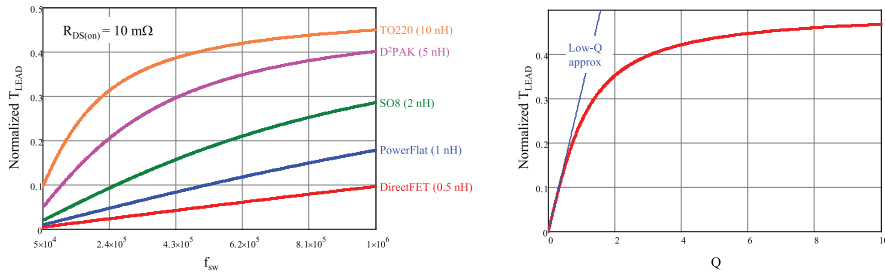


Figure 27.16: Normalized T_{lead} vs. switching frequency f_{sw} for different packages (left); normalized T_{LEAD} vs. Q of L_{stray} lossy inductor.

Note that if Q is sufficiently small, then $tan^{-1}(Q) \approx Q$, therefore T_{LEAD} can be approximated by:

$$T_{LEAD} \cong \frac{L_{stray}}{R_{DS(on)}}. \tag{27.4}$$

This is represented in the plot on the right-hand side of Figure 27.16 by the blue line. Eq. 27.4 provides an overestimate of T_{LEAD} not exceeding 10% as long as $Q < 0.569$.

Therefore, for a given $R_{DS(on)}$ the selection of the package is of crucial importance to determine the extent of the inductive early turn-off. The higher the switching frequency is, the more its stray inductance impacts on that. A package like the popular TO220 originates a significant T_{LEAD} even at low frequency, so it is inadequate for high frequency designs, where packages like DirectFET® or Powerflat^{TM} are preferred.

For a given package i.e., for a given L_{stray}, the lower the $R_{DS(on)}$ is the longer T_{LEAD} is, and this might limit the usage of very low $R_{DS(on)}$ MOSFETs and create the need of a tradeoff.

In any case, as much as the inductive early turn-off can be mitigated by appropriate design choices, normally it cannot be reduced to the point that its impact can be disregarded. Thus, it has become a common requirement for SR controllers to address this issue with the objective of making it negligible.

Now we will go through four of the most common strategies used in industry for minimizing the inductive early turn-off issue.

- Strategy one: RC compensation [20].

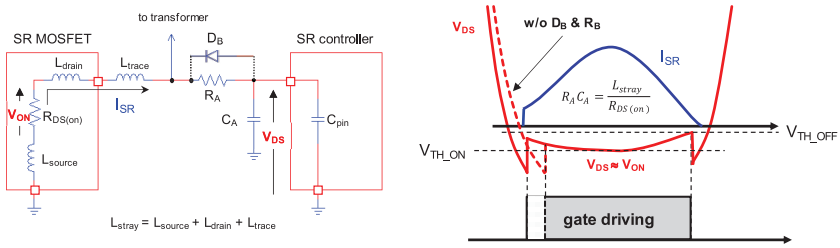


Figure 27.17: Inductive early turn-off compensation by RC circuit.

As illustrated in Figure 27.17, the signal for the V_{DS} sensing input goes through an RC low-pass filter (R_A, C_A). As usual, the SR MOSFET is turned off when V_{DS} exceeds the turn-off threshold V_{TH_OFF}.

If the time constant R_A C_A of the low pass filter equals the time constant associated to the lossy inductor, $L_{stray}/R_{DS(on)}$, the inductive early turn-off will be compensated.

The tolerance of $R_{DS(on)}$ and its changes with temperature limit the effectiveness of the compensation. Another shortcoming is that in practice the time constant needs to be tuned for the worst-case V_{DS} rate of rise, which occurs above resonance, where the last part of I_{SR} has a very high $\mathrm{d}i/\mathrm{d}t$. This means that at resonance and below resonance the inductive early turn-off will not be optimally compensated.

The simple addition of the RC low-pass filter delays not only the turn-off instant but also the turn-on instant because it delays and slows down the negative-going edge of V_{DS}, so that this will cross the turn-on threshold V_{TH_OFF} later.

This additional turn-on delay extends the duration of the conduction through the body diode, thus deteriorating efficiency. To minimize this additional delay a bypass diode R_B is backward connected in parallel to R_A. Its junction capacitance along with its low forward impedance will act as a speed-up.

The oscilloscope plots of Figure 27.18 show the effect of the RC compensation.

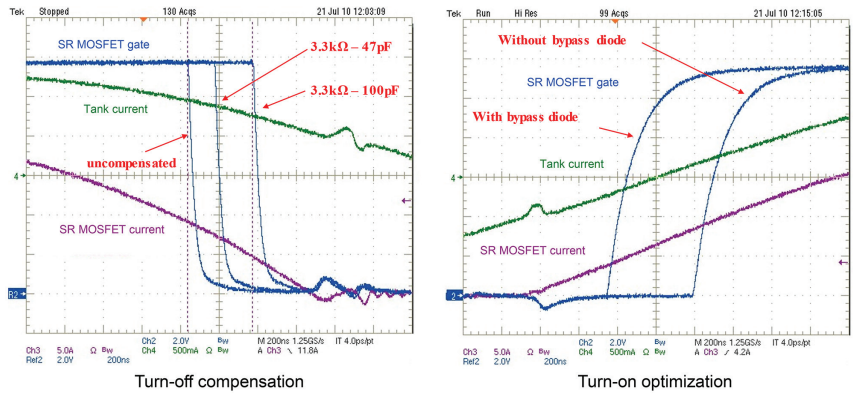


Figure 27.18: Inductive early turn-off compensation and turn-on optimization.

- Strategy two: V_{DS} regulation [60].

  With this technique, depicted in Figure 27.19, as V_{DS} exceeds a preset threshold V_{reg} (e.g., -30 mV), the gate-drive voltage is modulated to keep $V_{DS} = V_{reg}$ until the gate-drive voltage falls below the gate threshold or the current zeroes, whichever occurs first. Usually a turn-off threshold V_{TH_OFF} is provided anyway as a safety guard against current reversal. If V_{DS} exceeds V_{TH_OFF} the gate of the SR MOSFET is quickly pulled to ground with a low impedance switch.

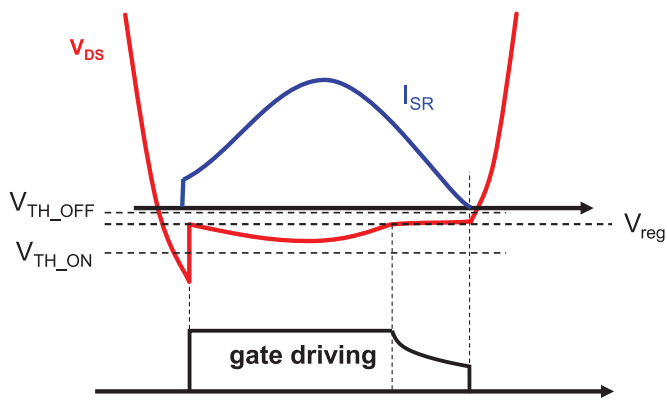


Figure 27.19: V_{DS} regulation principle.

The principle behind this approach is that as current approaches zero and the gate-drive voltage approaches the threshold of the SR MOSFET, its $R_{DS(on)}$ increases, thus T_{LEAD} is reduced, and the inductive early turn-off issue minimized. Additionally, the SR MOSFET can be switched off more quickly when current zeroes because the gate-drive voltage is close to the threshold.

- Strategy three: Adaptive turn-off [21].

  The control algorithm, graphically illustrated in Figure 27.20, minimizes the conduction time of SR MOSFET body diode after it turns off.

  Leveraging the inductive early turn-off, a turn-off delay is initiated from the instant when the zero-crossing of V_{DS} detected. This delay is updated cycle-by-cycle in small steps to obtain a body diode conduction time not exceeding a preset duration (e.g., 80 ns). Once the preset duration has been reached, The actual duration of the body diode conduction time jitters by one adjustment step around the target value. This residual conduction time is a safety margin against current reversal in case of changes in the operating conditions.

  A fast comparator referred to a slightly positive threshold prevents current reversal in case of fast transients.

- Strategy four: Stray inductance compensation [61].

  This technique considers an external compensation inductor L_{comp} (if its value is less than 10 nH, it can be realized with a PCB trace; rule of thumb: $L_{trace} \cong 7$ nH/cm), and a dedicated compensation input in the SR control IC, as shown in Figure 27.21.

  The source sensing input of the SR control IC represent the 0 V reference voltage; considering the direction of the secondary current $I_{SR}(t)$ the voltage drops across L_{source}, L_{drain}, L_{trace} and $R_{DS(on)}$ are conventionally negative, whereas the voltage drop across L_{comp} is positive. The voltage on the drain sensing input and that on the compensation input are internally summed and the resulting signal is compared to the turn-off threshold V_{TH_OFF}.

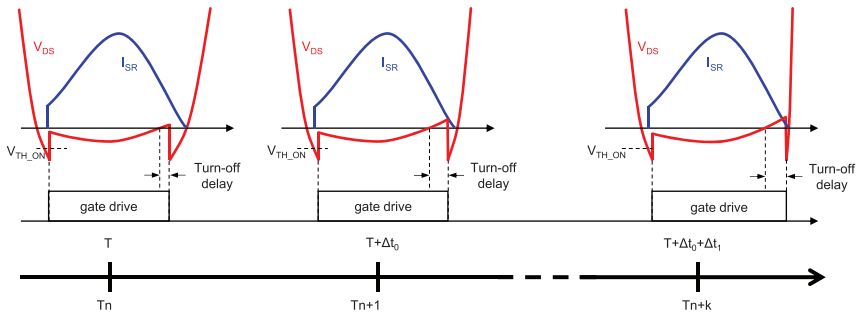


Figure 27.20: Adaptive turn-off principle.

If $L_{comp} = L_{source} + L_{drain} + L_{trace}$, the inductive drops are equal and cancel each other, so that the controller sees $V_{RDS(on)}$ only.

Printed Circuit Board Layout Hints

A proper PCB layout is essential for good operation of synchronous rectification. Below are a few hints that can help make a successful implementation. Figure 27.22 shows an example.

- Route the output current loop as short as possible by connecting the drain terminals of the SR MOSFETs as close as possible to the respective transformer "hot" terminations, and the source terminals close to the ground terminals of the output capacitor

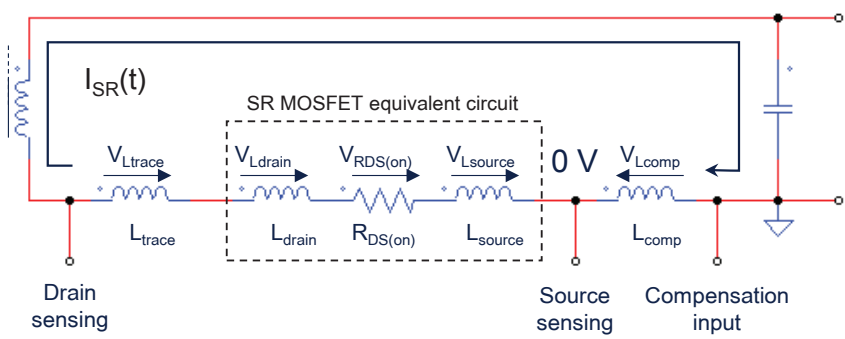


Figure 27.21: Stray inductance compensation operating principle.

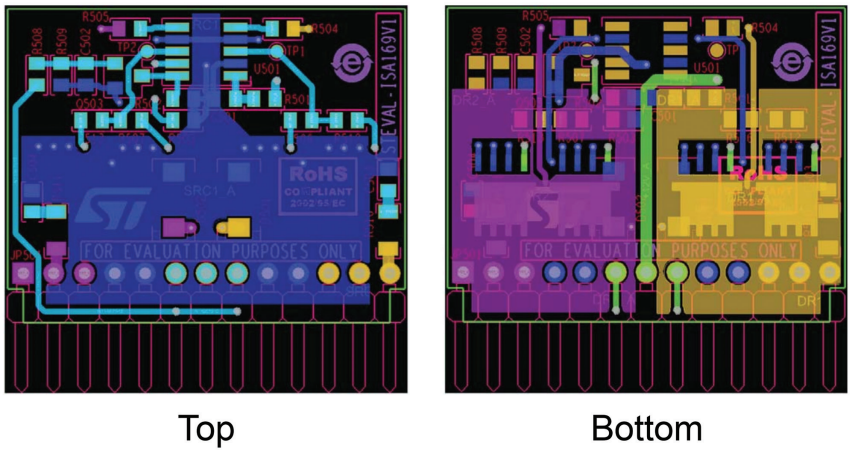


Figure 27.22: Exemplary PCB layout.

and as close as possible to one another. If the connection of the center tap to the positive terminals of the output capacitors cannot be short, consider bypassing it to ground with ceramic capacitors.

- Design the PCB and place the SR MOSFETs as more geometrically symmetrical as possible with respect to the transformer, to make circuit operation as electrically symmetric as possible. This includes routing the connection between the drain of the two SR MOSFETs and the transformer terminals symmetrically to one another.
- Use "Kelvin sensing" to sense V_{DS}, placing the connections as physically close as possible to the drain and source terminals of the SR MOSFETs.
- Route the trace that connects MOSFET sources to the ground pin of the control IC as short as possible and separately from the load current return path.
- Use bypass ceramic capacitors between the supply pin and the ground pin of the IC, located as close to them as possible.

- If the control IC has the ground pin that carries both the return of the device bias current and that of the gate drive currents, this ground pin should be routed to the common point where the source terminals of both SR MOSFETs are connected.

28

Interleaving of LLC Resonant Converters

Multiphase converters are a parallel combination of two or more switch-mode converters in any topology (typically the same for all), in a way that they share the same voltage source and provide power to the same load.

Multiphase converters are used when it is impossible or economically disadvantageous to comply with the design specifications with a single converter. The most common situation in which this approach is used is at a high power level: the total power demanded by the load is shared among a number N of converters, each one designed to carry 1/N of the total.

Very often in multiphase converters, control methods are actuated that essentially consist in staggering the pulse trains that control each converter in an appropriate manner. This is what is typically called *interleaving*. More specifically, interleaving consists in separating the signals used to drive each stage at the same frequency by some phase difference, with the total phase on all signals equal to 180° or 360°, according to the topology and design purpose.

With interleaving it is possible to provide a multiphase converter with properties that the individual converter does not possess.

Compared to single-phase converters, multiphase interleaved converters offer the following benefits:

(1) Multiphase converters extend the obtainable power range. Single-phase converters work well up to a certain amount of current, at higher currents power dissipation and efficiency start to become an issue. As previously mentioned, with an N-stage multiphase converter each individual stage manages 1/N of the total power, which reduces each stage's current to more manageable levels.

(2) Compared to a single-phase approach, in a multiphase converter the ripple current superposition at the input or the output results in a lower – sometimes theoretically zero - overall ripple and a lower ripple voltage across the input or output capacitors. The number of input or output capacitors and their ac ripple rating can be reduced.

(3) The differential-mode input or output EMI filtering requirements decrease in a multiphase converter due to the reduced ripple current.

(4) Compared to a single-phase converter carrying the total power, with the multiphase approach the size of the magnetic devices (inductor and transformers) are drastically reduced because of the lower rms current and saturation current requirements. The form factor of multiphase converters is generally better than that of a single converter carrying the same power.

(5) In multiphase converters the load transient performance can be improved. In the end, a system of N interleaved converters, each operating at a frequency f_{sw}, behaves as a single converter working at a frequency N $\cdot f_{sw}$, then potentially faster to react.

(6) In multiphase converters the efficiency can be kept very high on a broader load range resorting to the so-called *phase shedding*, i.e., shutting down the unnecessary phases when the load is low enough to be managed by a lower number of phases, and therefore reducing the losses associated to switching. For example, in a

system of three interleaved converters, one can be shut down when the load is lower than 2/3 of the full load, and a single converter can be left running when the load is lower than 1/3 of the full load.

Of course, the price to pay for these benefits is a greater system and control complexity, but this is normally worth the trouble.

It would be then very beneficial to adopt the multiphase approach in LLC converters too, especially when handling higher power levels (roughly, > 1 kW) or when there are special requirements on form factor or efficiency over a wide load range. In particular, LLC converters may benefit from using interleaving to reduce the output current ripple, which is one of their few drawbacks (refer to Table 4.1).

The bar chart in Figure 28.1 shows the theoretical output ripple amplitude reduction as a function of the number of phases. Compared to a single-phase converter, with two phases the ripple amplitude becomes about 1/5, with three phases about 1/11. Increasing the number of phases the ripple amplitude is reduced even further but the improvement

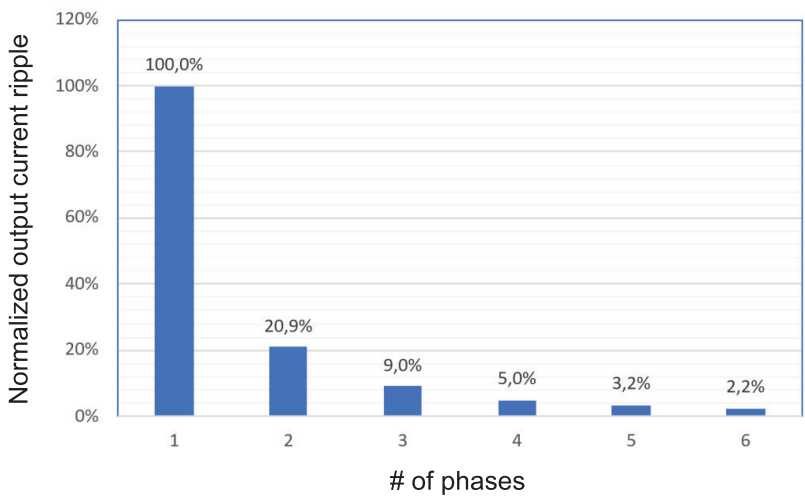


Figure 28.1: Output current ripple reduction in interleaved LLC converters vs. phase #.

becomes marginal while the system complexity and cost increase almost proportionally.

From the practical standpoint, special cases excluded, there is no point in going over 4 phases (which attenuate the ripple 20 times) and the majority of applications can be addressed with two and three phase interleaving.

While interleaving in PWM-controlled converters is relatively straightforward, this is not the case in resonant converters in general, and in LLC converters in particular. In fact, with the LLC converter *load sharing*, the capacity for the individual stages of equally sharing the current to be sourced to the load, is troublesome. This will be the focus of the discussion in this section.

Load Sharing Issue in Interleaved LLC Resonant Converters

Let us consider two nominally equal LLC converters that are paralleled with the intention of building a multiphase interleaved LLC converter. It is worth noting that to meet this goal, the output currents must be phase shifted by 180°; however, considering the frequency doubling effect of the secondary rectification (the secondary current has a periodicity of a switching half-cycle), the PWM pulse trains driving the primary-side switches must be phase shifted by 90°.

Despite nominally equal, the actual values of the parameters of the two resonant tanks (Ls, Lp, Cr) will not be the same, due to the tolerance of the physical components. Typically, Ls and Lp have 8–10% tolerance while Cr can be selected in a 5% tolerance series. Tighter tolerances entail a part selection (binning) to exclude those parts that are out of the desired tolerance band. This practice is typically not recommended in mass production because it is expensive and time consuming.

The effect of these tolerances is that the two tank circuits will have different resonance frequencies f_{R1}, f_{R2}. It is possible to deduce the consequences of this difference based on the FHA model of the converters and using the plot of the voltage gain $|M(x, k, Q)|$. To do so, let us refer to the diagrams of Figure 28.2 that illustrate the effects

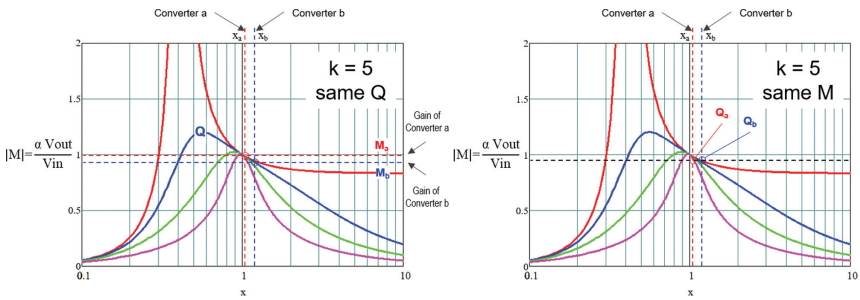


Figure 28.2: Gain mismatch due to tolerance of tank circuits in LLC converters.

of the mismatch of f_{R1}, f_{R2}, assuming for simplicity that the ratio $k = Lp/Ls$ is unchanged.

Interleaved converters operated at the same frequency f_{sw} (they must be, to keep a fixed phase difference) have different normalized frequencies ($x_a = f_{sw}/f_{R1a} \neq x_b = f_{sw}/f_{R1b}$), thus they have different dc gains M_a, M_b if operated with the same Q (i.e., the same load), as shown in the $|M|$ plot on the left-hand side. This violates the initial assumption of paralleled converters, which have the same input and output voltage.

Vice versa, if operated with the same voltage gain M as shown in the $|M|$ plot on the right-hand side, they have different Q values, Q_a, Q_b. Consequently, the converter with a higher gain has a higher Q and delivers the most power, the other may be even nearly unloaded.

For a better understanding of the issue, and with the aim of developing some design guidelines to help minimize the effects of the component tolerance on load sharing, it is interesting to analyze the impact of the tolerance of the individual components. This analysis is reported in [30] and can be synthesized in the following points:

- The mismatch of the upper resonance frequencies f_{R1a}, f_{R1b} has by far the largest impact. The reason is the low output impedance in the vicinity of the upper resonance frequency, where the voltage gain is unity (load-independent point).

- The impact of the parallel inductances Lp_a, Lp_b mismatch is small in the above resonance operation, more accentuated in the below

resonance operation. This is consistent with the fact that the lower resonance frequency f_{R2}, which is associated to Lp, shows up in the below resonance operation only.

- The characteristic impedance mismatch (i.e., the mismatch of the Ls/Cr ratio) has a small impact under all operating conditions.

To get a quantitative idea, [30] reports that in a 2-phase interleaved LLC converter, assuming that the tolerance of Ls, Lp, Cr is $\pm 2.5\%$ for all of them (which is possible in mass production only using binning), the worst-case load sharing error is larger than $\pm 20\%$ when operating at resonance at full load, and the sharing error gets even higher at lower output loads.

From a practical point of view, it is important to have a good load current sharing between phases when their mismatch degrades converter characteristics or performance, or causes significant stress or thermal differences that in the long run may cause reliability issues.

For example, unequal load sharing causes a larger output current ripple (see Figure 28.3) that, in turn, causes a larger output voltage ripple and an increase in stress on the output capacitor bank. This means that load sharing is critical especially at heavy and intermediate load. In a system with phase shedding, good load sharing should be ensured down to a power level where a single phase remains active.

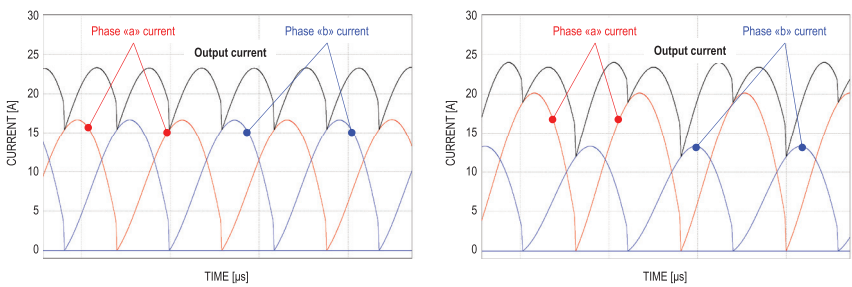


Figure 28.3: Secondary currents superposition in a 2-phase interleaved LLC converter: no mismatch (left), 2.5% mismatch of resonant capacitors (right).

This high sensitivity of load sharing performance to component value mismatches prevents the use of multiphase interleaved LLC converters

without some workaround. It is worth mentioning that power losses act as a balancing element and an analysis made taking them into account shows that load imbalance is smaller than one would expect using simpler ideal models. However, it makes little sense to denature the high efficiency property of the LLC converter to enable a better load sharing.

The question is then how to compensate for the resonant tank mismatch and force phases to share load current equally (current balancing).

As previously mentioned, the frequency of the V_{HB} square wave applied to each tank current must remain the same for all phases, otherwise the superposition of the currents of each stage will continuously oscillate at the beating frequency. In principle, the duty cycle of V_{HB} could be moved from 50% to increase the converter's gain, but doing so is not recommended because it will simply shift the problem elsewhere: from load current imbalance between phases to current imbalance in the two half-cycles of the duty-modulated converter.

We need an extra degree of freedom, like in a full bridge where the phase-shift of the two switching legs can be used for this purpose.

Considering 2-phase interleaved LLC half bridges, it is possible to mitigate the effects of mismatch with an appropriate design of the tank circuits (passive method). For a significant reduction of the effects of mismatch, one should consider some active method.

Considering 3-phase interleaved LLC half bridges, self-balancing topologies exist and an example will be given in the following discussion.

Designing Tank Circuits for Interleaving

To mitigate the effects of tank circuit mismatch on load sharing, the individual converters should be designed so that their dc gain does not change much in case of f_{R1} mismatch that, as stated in the previous section, is the major responsible for unequal load sharing.

In addition to that, it is intuitive that the more converters tend to behave as voltage sources, the more the effects of their mismatch increase: just think of what happens when trying to parallel voltage sources. Therefore, the individual converters should be designed to behave more

as current sources i.e., designed for a higher output impedance *Zout* and to be operated in a frequency region where the output impedance *Zout* is higher. The FHA analysis can provide some insight.

Firstly, looking at the plot of $|Zout|$, on the left-hand side of Figure 28.4, the individual converters should not operate at resonance, where *Zout* is theoretically zero (low in real-world operation).

Looking at the plot of $|M|$ on the right-hand side of Figure 28.4, all $|M|$ curves cross the load-independent point (1, 1) with a $-2/k$ slope; around that point, curves with Q larger than a certain value (roughly corresponding to the blue curve) have a lower slope below resonance and a higher slope above resonance.

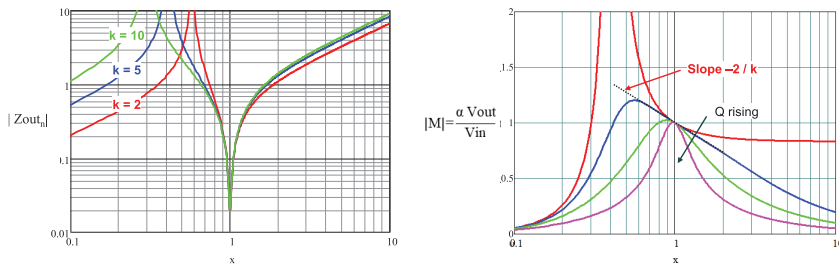


Figure 28.4: $|Zout_n|$ plot and $|M|$ plot suggest design rules to mitigate mismatch effects.

Therefore, based on these observations, the tank circuit should be designed according to the following three guidelines:

- To minimize the impact of f_{R1} mismatch, the tank circuit should be designed with a low $|M|$ curve slope, then a high $k = Lp/Ls$, but with some care (see the last point).
- To achieve a higher *Zout*, the tank circuit should be designed with a high characteristic impedance $Z_0 = (Ls/Cr)^{\frac{1}{2}}$ (i.e., high Ls, low Cr).
- Since $Q = Z_0/Rac$, a high Z_0 implies a high Q; to reduce the slope of the $|M|$ curve with increasing Q, the converter must be operated below resonance. Notice that with higher k values the rate of rise

of the output impedance *Zout* with decreasing frequency in the below operating region gets smaller. Then k should be increased as long as the benefit of a lower slope of $|M|$ prevails on the lower *Zout* rate of rise.

This approach, however, has some significant shortcomings, specifically:

- Working away from resonance worsens efficiency in nominal conditions: operating always in DCMB mode below resonance involves a worse form factor of both the primary and secondary currents, leading to higher conduction losses.
- Each converter will work closer to the capacitive mode region. Care must be taken to safely handle out of spec operating conditions (e.g., an input voltage lower than the minimum specified).
- Ultimately, the load current mismatch is mitigated but still significant; as a result, each converter must be designed for a power considerably larger than their theoretical share of the total power.

Active Interleaving in 2-Phase Interleaved LLC Half Bridge Converters

Several current balancing methods have been proposed to solve the load sharing issue. In this section some of these methods, referred to 2-phase systems, will be reviewed.

- Series-parallel connection [51], [52]

  With this technique, the input voltage is split by two capacitors and fed to the two phases connected in series. The outputs are connected in parallel, as shown in Figure 28.5.

  This arrangement provides an intrinsic negative feedback that improves load sharing, though not fully equalizing the individual currents.

  Its operating principle can be explained considering that, if one phase has a higher dc gain, that phase will provide more power and its input capacitor will be discharged more; the voltage on the

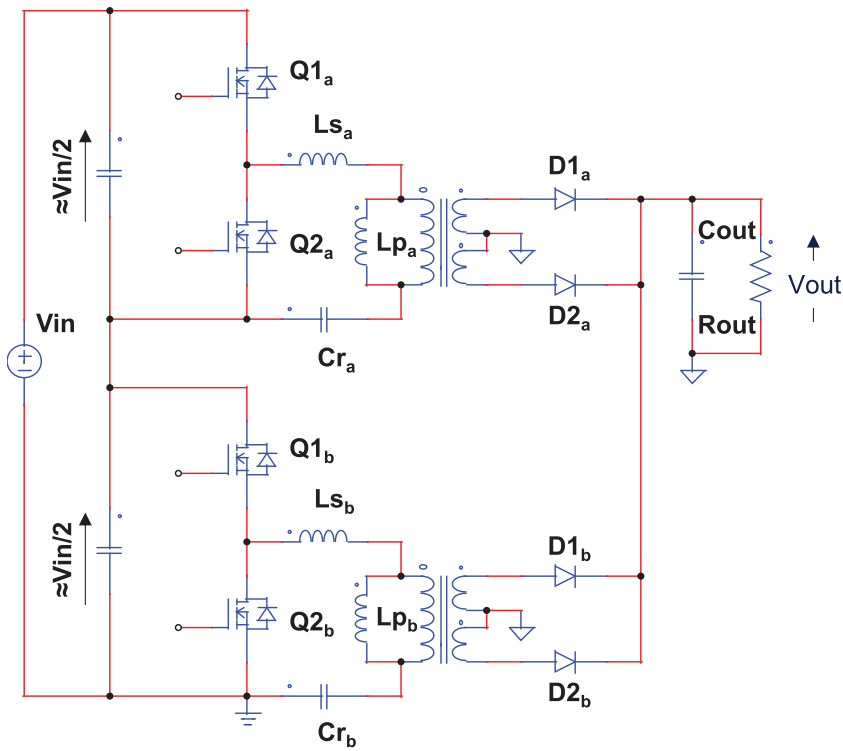


Figure 28.5: Series-parallel connection of a 2-phase interleaved LLC converter.

capacitor of other stage will increase accordingly because the sum of the two voltages must equal *Vin*. This input voltage imbalance contrasts the dc gain mismatch and the resulting load current mismatch will be reduced.

Unfortunately, this technique has a couple of non-negligible drawbacks. Firstly, the input voltage of the individual phases is halved, so the input current is doubled, as if it was a single-phase converter. Conduction losses will be higher, efficiency will be impaired. Secondly, phase shedding is not possible: in fact, if one phase is shut down there is no dc path for the input current. From a different angle, the negative feedback mechanism that tends to balance currents pushes the input capacitor voltage of the disabled phase

(which carries no power) to the maximum (Vin), discharging the completely the other, whose voltage goes to zero.

- Separate supply rails [30]

  With this solution, illustrated in Figure 28.6, each LLC converter is powered by a separate dc-link voltage generated by two separate PFC stages.

  A current balancing loop adjusts the output voltage setpoint of one PFC stage (or both), so that $Iout_a$ and $Iout_b$ are equal to one another: $Iout_a = Iout_b = Iout/2$.

  The main drawback of this technique is the system complexity and cost. However, it is a viable solution in high power converters that use an interleaved PFC front-end. In this case there is no significant increase in complexity, but the ripple cancellation on the output bulk capacitor is lost. This is often acceptable because largely repaid by the benefit on the most stressed components, the output capacitors of the LLC converter.

- Current-controlled inductor [65]

  With this approach, as illustrated in Figure 28.7, two additional inductors are added on the primary side: a fixed value inductor (L_F) is in series to the tank circuit of one phase and a current-controlled inductor in series to the tank circuit of the other phase. The purpose of the variable inductor is to equalize the upper resonance frequencies of the two tank circuits and, ultimately, equalize the currents of each phase.

  The variable inductor is built as conceptually illustrated in Figure 28.8 (left). The N_L turns on the center post of the core are used to obtain L_{sat}, while two series-connected windings of N_S turns each wound on the outer legs of the core make the control winding that is used to modulate L_{sat}.

  This modulation is achieved by forcing a dc-current (control current, I_{CTL}) through the control winding. This causes the core to slightly saturate, therefore changing its effective magnetic permeability and thus modulating the value of L_{sat}: The higher I_{CTL} is,

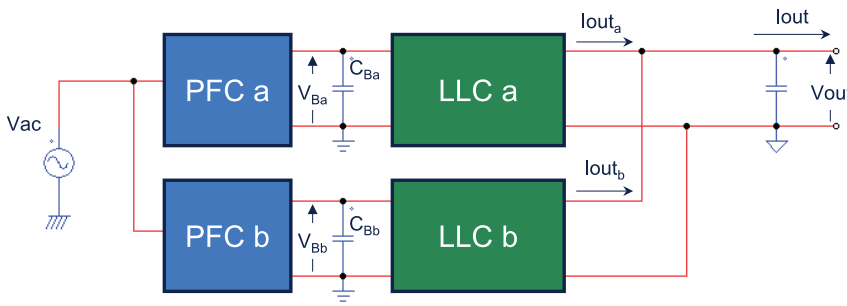


Figure 28.6: Dual dc-link configuration of 2-phase interleaved LLC converter.

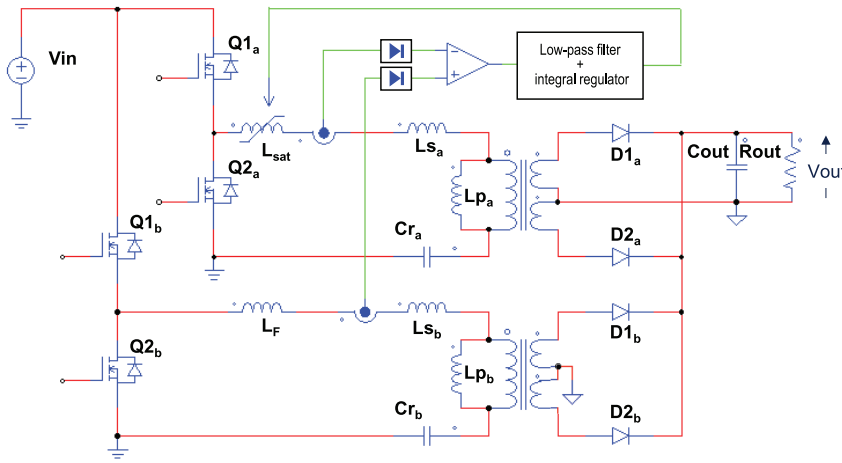


Figure 28.7: Load current balancing in a 2-phase interleaved LLC converter through a current-controlled inductor.

the lower L_{sat} will be, as shown in the plot on the right hand-side of Figure 28.8.

The adjustment of L_{sat} goes in one direction only, whereas it is necessary to adjust in both directions because the sign of the mismatch is not known. This requires the addition of the fixed inductor L_F, whose value will be chosen roughly in the middle of the adjustment range of L_{sat}. An alternative approach like purposely imbalance the leakage inductance of one transformer to predefine the needed adjustment direction, (i.e., embedding L_F

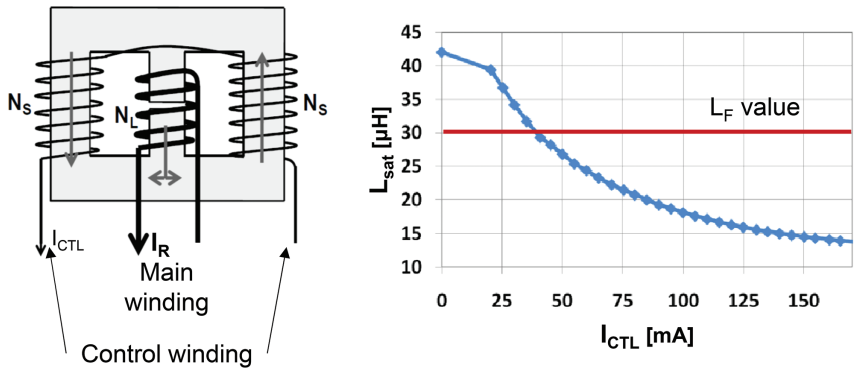


Figure 28.8: Current-controlled inductor and L_{sat} vs. I_{CTL} relationship.

in its leakage inductance) would require the use of different transformers for the two phases, which is not usually a recommended practice.

Though the system works effectively, the addition of two magnetic parts, as well as of the current balancing regulator, increases system cost and size.

One aspect needing attention is the power consumption associated to the current balancing regulator, which will degrade converter's efficiency. This can be minimized by using a large turns number N_S to reduce the amplitude of I_{CTL}, and keeping the voltage source that produces I_{CTL} as small as possible.

Using phase shedding the controlled phase can be shut down at light load along with the current balancing regulator, which therefore will not affect light load efficiency.

Notice that in the system of Figure 28.7, the current balancing loop is based on the comparison of the resonant tank currents of the two phases. This provides a good output current balancing as long as the magnetizing current is negligible compared to the total resonant current, i.e., at medium and heavy load. At light load the tolerance of Lp worsens current balancing significantly. To improve this behavior, the secondary currents should be sensed instead. Since in interleaved systems the output current is normally high,

the introduction of additional losses due to sensing might be an issue. Additionally, in primary-controlled systems current sensors should transfer the signal from the secondary to the primary side, so they should guarantee safety isolation.

- Switch-controlled capacitor [43]

  This approach, shown in Figure 28.9, can be considered conceptually the dual one of the current-controlled inductor method: to match the upper resonance frequencies of the two tank circuits, the effective value of the resonant capacitor is modulated.

  This is achieved by modulating the duty-cycle of the switches S_a, S_b. With reference to Figure 28.10, first harmonic analysis shows that the effective capacitance value, Ca_e, is a function of the control angle α:

$$Ca_e = \frac{2\,Ca}{2 - \frac{2\alpha - \sin 2\alpha}{\pi}}. \tag{28.1}$$

  Ca_e goes from Ca when $\alpha = 0$, i.e., when the switch S is always off to ∞ (a short circuit can be assimilated to an infinite capacitance) when $\alpha = \pi$, i.e., when S is always on.

  As a result, the overall resonance capacitor Cr goes from Cr when the switch S is always on, to the series combination of Cr and Ca when the switch S is always off. Of course, Ca will be selected so as to cover all the necessary adjustment range. Normally, it needs to accommodate small variations, so its value is not much different from that of Cr, sometimes it is even larger. This is a favorable fact because the peak voltage across Ca will not be that high and lower voltage rating MOSFETS can be used as the switch S.

  To minimize switching losses, S is operated with ZVS at turn-on: S is turned on when its drain-source voltage falls to zero after the positive peak. S is turned off when the control angle α programmed by a current balancing loop has been reached. Notice that the angle α is counted starting from a positive-going zero-crossing of the tank current. Digital control is practically a must.

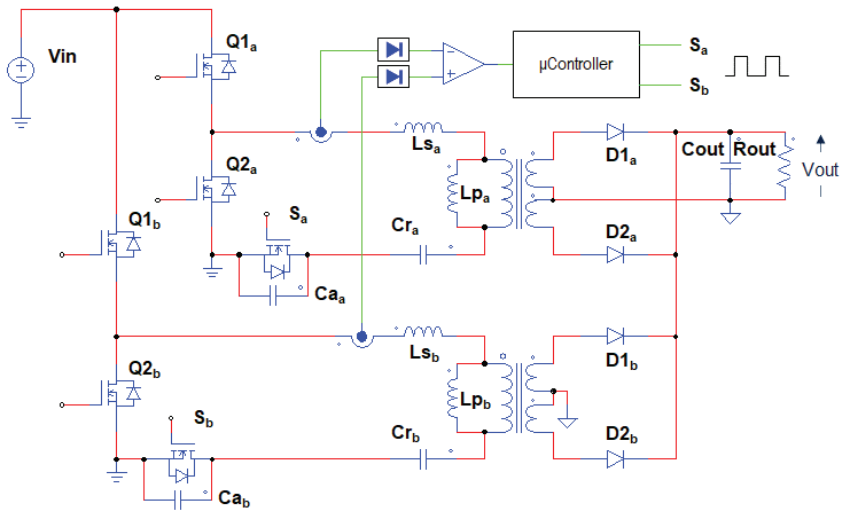


Figure 28.9: Load current balancing in a 2-phase interleaved LLC converter through switch-controlled capacitors.

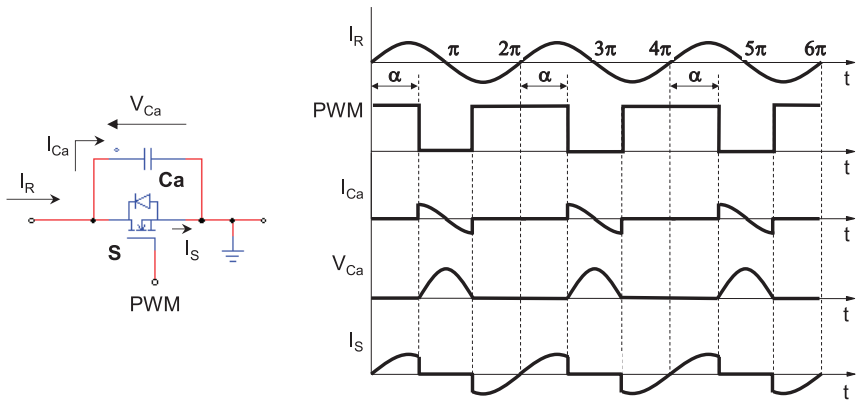


Figure 28.10: Structure (left) and key waveforms (right) of a switch-controlled capacitor.

Three-Phase Interleaved LLC Converters – An Example

For power levels in the range of kW one could consider splitting the load power in more than 2 phases to optimize the design of each individual phase. Among the many three-phase interleaved LLC converters that

have been described in the literature [8], [36], [56], [63], [64], we will review one particular solution, based on the use of three LLC converters with a Y connection of the tank circuit [63], [64].

Differently from other multi-phase solutions that are greatly sensitive to resonant components' tolerance causing current imbalance, this topology exhibits an inherent load sharing capability. Should its native balancing ability not suffice to meet the design requirements, a closed-loop phase-shift control can be implemented to compensate for the residual current mismatch and completely balance the current supplied by each phase.

The schematic of this topology is shown in Figure 28.11. A version with single-ended secondaries and a three-phase bridge rectification is shown in Figure 28.12.

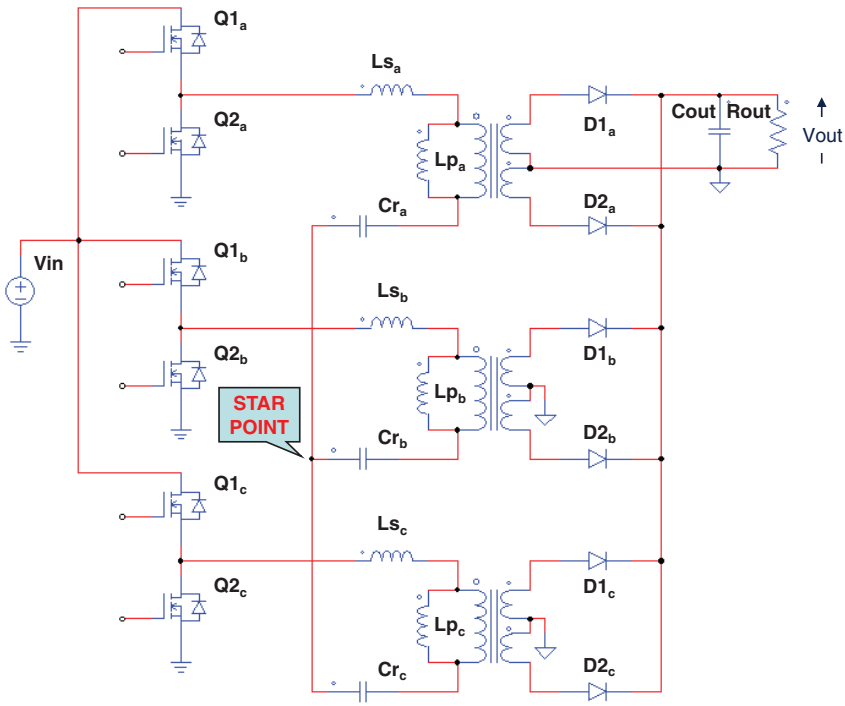


Figure 28.11: Three-phase interleaved LLC converter with Y connection of tank circuits and FW-CT secondary rectification.

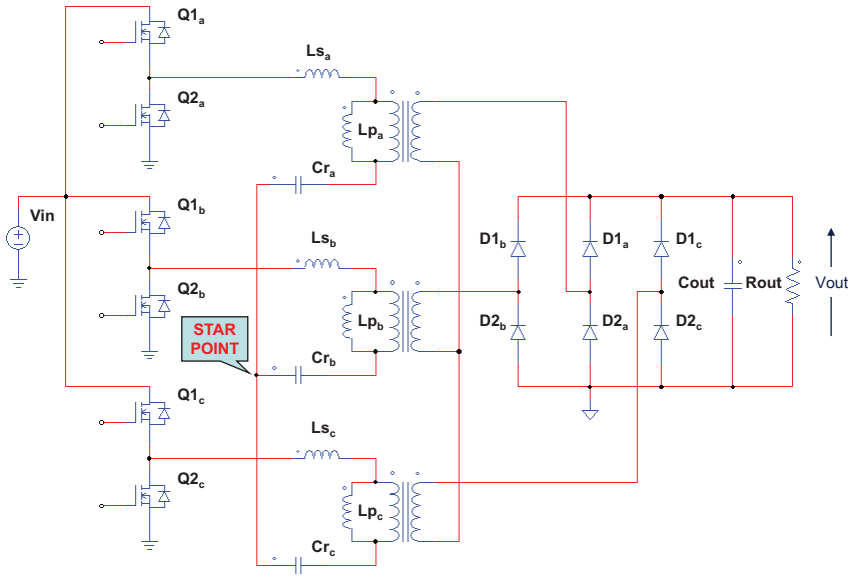


Figure 28.12: Three-phase interleaved LLC converter with Y connection of tank circuits, single ended secondaries and three-phase bridge rectification.

The floating star point that connects all the three tank circuits provides the degree of freedom that enables the three converters to run at the same frequency with 120° phase-shift between each phase and equally share the overall current. The interesting property of this topology is that the voltage of the floating star point moves so as to automatically balance the currents in each phase.

The oscilloscope picture on the left-hand side of Figure 28.13 shows the tank current in each phase of a 3-phase prototype loaded with a total output current of 24 A, with their natural mismatch. The deviations of the individual output currents from the target value (8 A) are +5% in phase a and –2.5% in phases b and c. On an extreme level, on the right-hand side the same waveforms are shown after increasing the value of Cr_c by 12%. The deviations from target are now –6.25% in phase a, +8.75% in phase b and –2.5% in phase c.

The results of the same measurements done with the star point grounded, so that the three phases are simply paralleled, are shown in

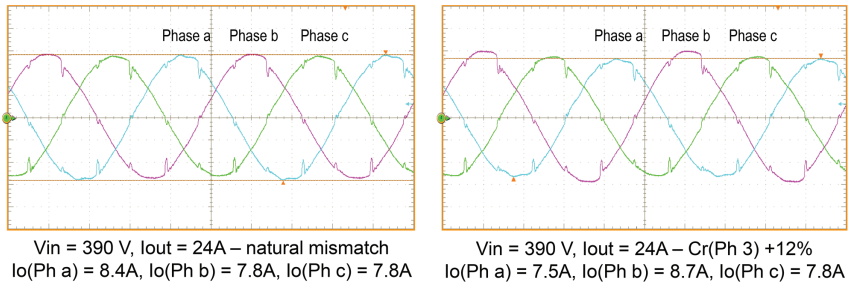


Figure 28.13: Resonant currents in a three-phase interleaved LLC converter with Y connection (star point floating).

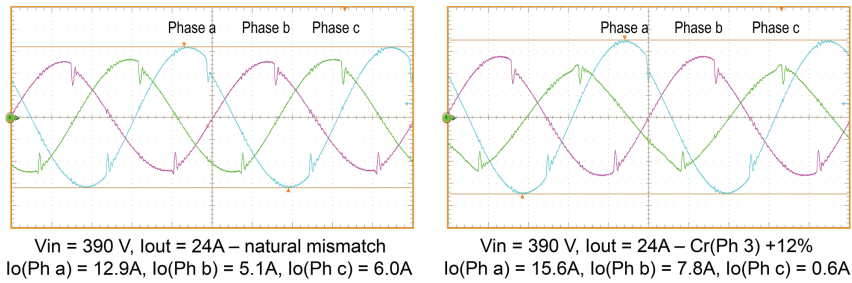


Figure 28.14: Resonant currents in the same three-phase interleaved LLC converter with star point grounded.

Figure 28.14. Now the deviations of the individual output currents from the target value (8 A) with the natural mismatch are +61% in phase a and –36% in phase b and –25% in phase c. Increasing the value of Cr_c by 12% the deviations from the target become +95% in phase a, –2.5% in phase b and –92.5% in phase c.

The benefit of the floating star connection is dramatic. In a system where a ±10% mismatch in the individual output currents is acceptable, there is no need for current sharing control. In case of more stringent requirements, a current balancing loop can be closed that acts on the phase-shift between phases to equalize the individual currents.

With this loop the individual current can be balanced to less than 5% [64] down to about 1/3 of full load with a primary current sensing. As to this accuracy and possible improvements, the same comments made

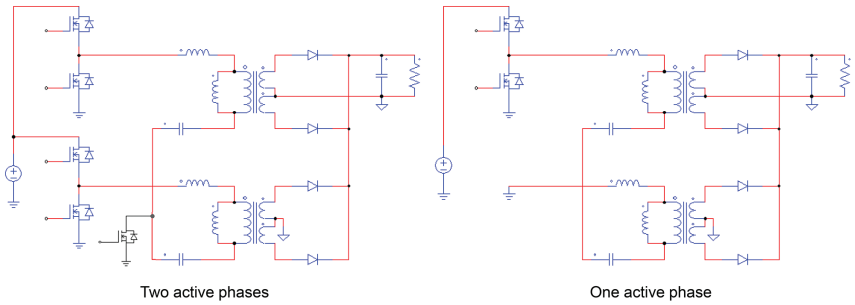


Figure 28.15: Three-phase interleaved LLC converter with Y connection: phase shedding.

about the current balancing loop in the current-controlled inductor method apply also here.

The floating star point brings current balancing but unfortunately prevents the traditional phase shedding, where one phase is simply shut down and the phase-shift between the remaining phases properly adjusted (from 120° to 90° going from three to two active phases).

Figure 28.15 (left-hand side) shows two possible 2-phase configurations obtained by shutting down phase c. If both MOSFETS $Q1_c$ and $Q2_c$ are kept off and the phase-shift of the driving signals of phase b changed from 120° to 180° (with respect to phase a), phase a and b become a full bridge sharing the series of their tank circuits.

Using an auxiliary switch that is turned on connecting the star point to ground when phase c is shut down, the two active phases are actually paralleled. Changing the phase-shift of the driving signals of phase b from 120° to 90° a traditional interleaving between phases a and b is possible but with no inherent load sharing property, with all the issues previously described.

Figure 28.15 (right-hand side) shows a possible single-phase configuration resulting from shutting down phases b and c. To provide a return path for the resonant current, however, the low-side MOSFET of phase b is kept on. The tank circuits of phases a and b therefore in series and operated as a single half bridge converter. Notice that it is not a true single-phase operation because the components of two phases are involved in current conduction.

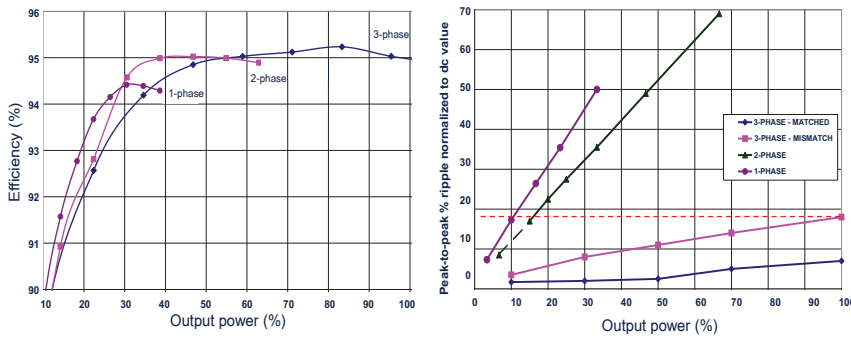


Figure 28.16: Efficiency (left) and output ripple (right) vs. load and phase shedding in a three-phase interleaved LLC converter with Y connection.

When going from three to two active phases the output current ripple increases significantly: either the system turns to a single full bridge, in which case there is no staggering of the secondary currents, or is a 2-phase interleaved system where the individual currents can be even heavily imbalanced.

When going from two to one active phase, of course there is no possible ripple reduction but this happens at light load and the resulting ripple is low, presumably less than the ripple at full load with three active phases.

The issue is then at intermediate loads, where a trade-off between efficiency improvement and output current ripple is necessary. Figure 28.16 shows the plots of efficiency vs. load and output ripple vs. load for the same 3-phase converter whose waveform were shown in Figures 28.13 and 28.14, to get a quantitative idea of the compromise.

29

Topology Variants

LLC converters, like essentially all power converters, can be modified to enhance certain characteristics or to more easily meet some specific design requirements.

Some simple examples of these so-called topology variants have been encountered already during the present discussion: for example, the half bridge and the full bridge versions, the split-capacitor version (see Figure 4.4) or the various configurations of secondary rectification (see Figure 3.4).

Many topology variants have been proposed in the literature over the years [13] and the extension of the application range in power and the continuously increasing performance demand is driving further evolutions. A few topology variants that are in use in industry will be overviewed in this section. For a deeper analysis, readers are referred to the related literature.

Two-Transformer LLC Converter

This topology variant, shown in Figure 29.1 in its half-bridge version, can be found in some high power (e.g., server power) or slim designs (e.g., flat TV SMPS [50]). Two transformers are connected with the

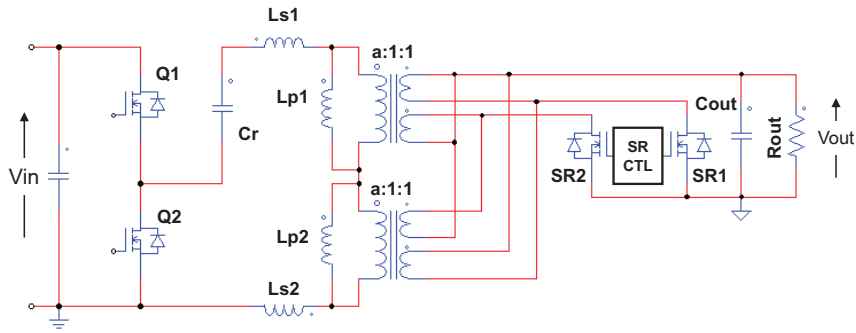


Figure 29.1: Two-transformer half bridge LLC converter (version I).

primary windings in series and the secondary windings in parallel. The series connection of the primary windings ensures equal current sharing between the two transformers. The operation is essentially the same as that of a conventional HB or FB.

The schematic of Figure 29.1 shows a CT-FW rectification configuration but the SE-B can be used too as in [50]. Synchronous rectifiers are considered because this topology is normally employed in power-dense applications with a high output current, as previously mentioned.

Notice in Figure 29.1 the cross-connection paralleling of the secondary windings, an expedient to minimize the asymmetry of the secondary currents due to the unavoidable transformer asymmetries.

Comparing the characteristics of each transformer to those of a single transformer designed for the same application, since the voltage applied to the primary winding of each transformer is half the voltage applied to the entire inductive section of the LLC tank, all its parameters (a, Ls, Lp) are cut in half.

Due to the parallel connection on the secondary side, the voltage seen by each secondary is the same output voltage, so each transformer can be designed with the same secondary volt per turn. Therefore, the number of secondary turns does not change and the number of primary turns is cut in half. Furthermore, since each secondary winding carries half the total output current, the cross sectional area of the secondary windings can be cut in half too.

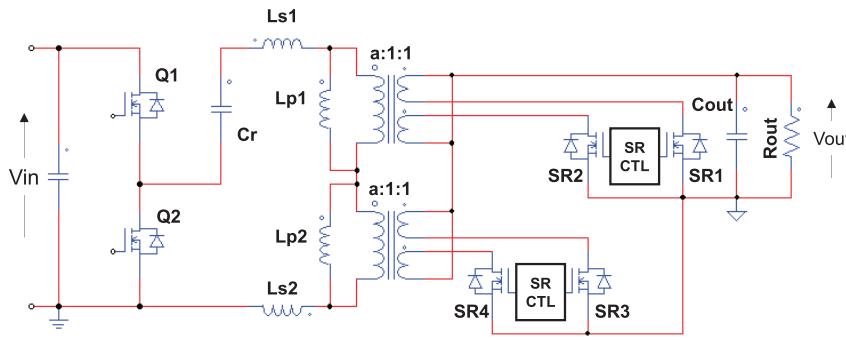


Figure 29.2: Two-transformer half bridge LLC converter (version II).

It is possible to reduce the size of each transformer because of a reduction of the core window area, and thus achieve a higher power density.

Figure 29.2 shows a different version of this topology, where each transformer has its own secondary rectification and paralleling occurs after the rectification blocks. Also in this case the converter can be an HB or a FB and the secondary rectification configuration CT-FW or SE-B. In [81], for example, the converter is a FB with a dual SE-B rectification.

This version definitely requires more external parts and is therefore more expensive. However, although it might appear less efficient too, it is not necessarily so. The parallel connection after the rectifiers prevents possible current flow, due to transformer mismatch, that may occur in the current mesh that exists in the version of Figure 29.1 as a result of the connection of the secondary windings before the rectifiers.

LLC Converter with Matrix Transformer

LLC converters with matrix transformer can be considered to be a generalization of the two-transformer LLC converter shown in Figure 29.2.

By definition, as reported in [37], a matrix transformer is an array of smaller parts called *elements* properly interconnected so that the whole functions as a single transformer. Each element is a single small transformer with a preset turns ratio (e.g., 1:1, 2:1, etc.) and the desired

turns ratio is achieved by connecting the primary windings of the elements in series or parallel and the secondary windings in series or parallel, depending on the design objective. In our case of converters operated off the power line and required to deliver a relatively high current, the most appropriate combination is to connect the primary windings in series and the secondary windings in parallel.

Matrix transformers offer significant benefits: they can split a large current between the parallel-connected secondary windings, reduce the secondary-side leakage inductance by lowering the number of secondary turns (1 turn is quite common in high output current applications) and improve the overall thermal performance by distributing the power loss throughout the various elements. Additionally, with appropriate interleaved structures matrix transformers can significantly reduce the magnetomotive force (MMF) of the windings, thus reducing leakage inductance and winding ac resistance due to skin and proximity effects, which is particularly advantageous in high switching frequency applications.

Matrix transformers find their construction of choice using planar magnetic cores and with windings realized on a multilayer PCB that accommodates also the rectifier block (SR will be used for high efficiency) and the output capacitors bank to minimize leakage and termination loss.

Figure 29.3 shows the secondary-side of an LLC converter with matrix transformer as reported in [44], where a single big transformer is replaced by four smaller transformers. Comparing the characteristics of each transformer to those of a single transformer designed for the same application, all its parameters (a, Ls, Lp) are reduced four times. Also, the number of primary turns will be four times smaller.

The drawback of this approach is that a magnetic ferrite core is required for each elementary transformer. Reference [26] reports a different matrix transformer structure that integrates multiple transformers into a single magnetic core as schematically shown in Figure 29.4.

This approach utilizes flux cancellation to reduce flux density in the magnetic limbs and the relevant core losses. Additionally, it does not require a PCB with a large number of layers, thus offering a considerable cost reduction compared to a multi-core matrix transformer.

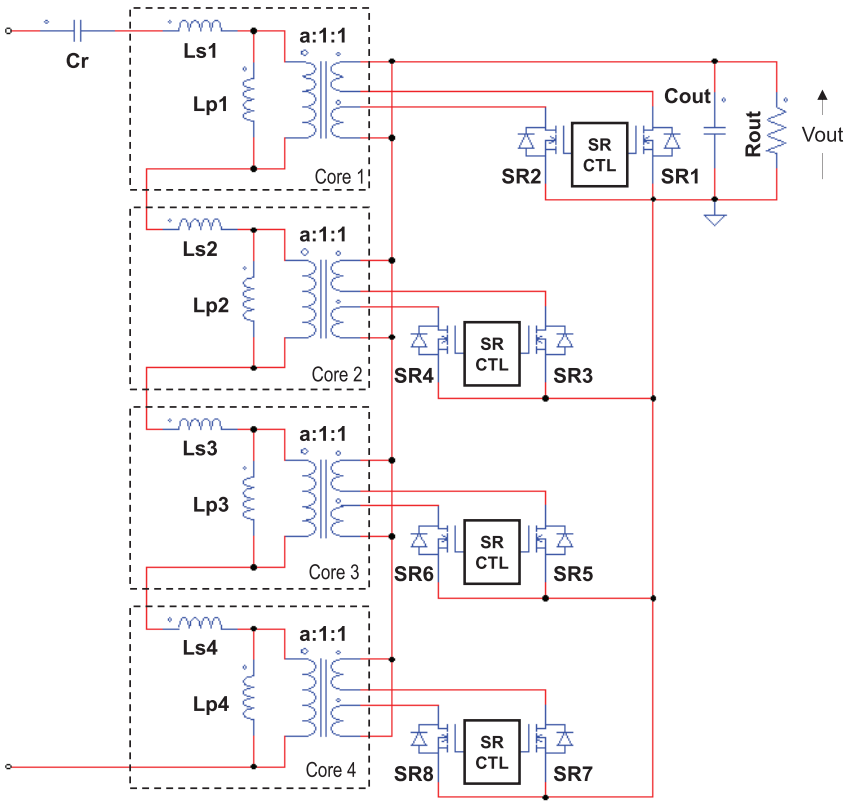


Figure 29.3: Tank circuit and output stage of an LLC converter with matrix transformer.

Three-Level LLC Converter

The multilevel approach can be considered as the dual of the multiphase approach: while in multiphase converters the switch structures are essentially connected in parallel, in multilevel converters the switch structures are stacked on top of each other. Compared to a multiphase approach, which requires a magnetic device per each phase, in multilevel converters a single magnetic device is generally needed.

This technology has been used widely in railway systems, ship electric power distribution systems, fuel cell systems, renewable energy systems (photovoltaic and wind turbine) and other high-voltage systems,

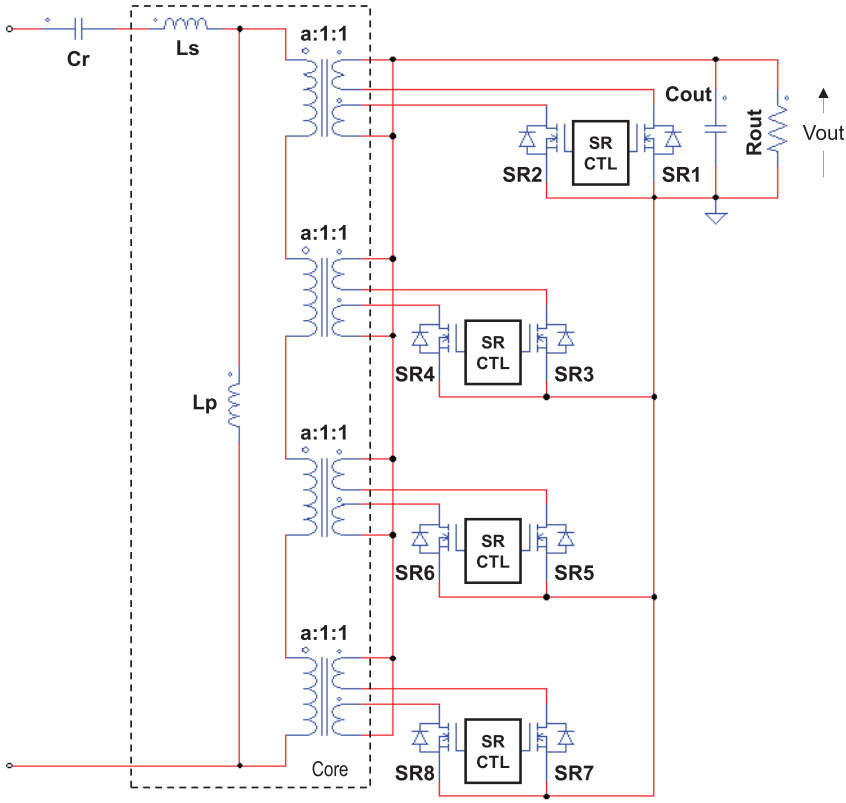


Figure 29.4: Tank circuit and output stage of an LLC converter with a single-core matrix transformer.

e.g., those operated from medium voltage distribution lines or the three-phase line. In fact, its fundamental benefit is that the voltage across each switch is reduced proportionally to the number of levels.

Therefore, high voltages can be handled with moderate voltage rating switches, which generally perform better than high-voltage devices. Consider, for example, that the die area necessary to achieve a given $R_{DS(on)}$ increases with the voltage rating following a power law with an exponent greater than 2. A larger die size to withstand higher voltages means not only more expensive switches, but also switches with larger parasitic capacitances that are harder to drive and have larger losses.

In addition, the multilevel approach reduces the voltage swing that switches undergo, thus reducing not only conduction losses due to a lower $R_{DS(on)}$ but also switching and capacitive losses. As a positive side effect, this produces less common-mode voltage, thus reducing the EMC issues.

In particular, considering three-level systems, the voltage rating of the switches can be half the input voltage.

This property could be used the other way round in offline applications, i.e., handling input voltages that are normally handled by conventional converters with multilevel converters, using lower voltage switches featuring a much lower $R_{DS(on)}$. Unfortunately, using only three level is not a viable solution. Today 600 V devices are commonly used in a conventional half bridge (or a full bridge) operated from a 400 V input voltage bus provided by a PFC pre-regulator. With three levels one could use 300 V rated devices and this is a voltage area where there has been not much industry focus: few part numbers are available and the technology has not been extensively developed like for higher or lower voltage parts. One more level should be added to use 150 V rated devices, where the technology actually offers a significant $R_{DS(on)} \times$ die area reduction.

This, however, emphasizes the biggest drawback of this approach: the need for a great number of switches (4 with a three-level converter, 6 with a four-level converter and two more for each additional level), each requiring a related gate-drive circuit (all floating except one). This may cause the overall system to be more expensive and overly complex.

A three-level LLC resonant converter is illustrated in Figure 29.5. It consists of two stacked half bridges and the resonant tank is connected to the two midpoints.

In the most straightforward driving scheme, Q1 and Q4 are turned on and off simultaneously and so do Q2 and Q3. The advantage of this scheme is that it can be readily implemented using any commercially available resonant controller IC with the addition of two gate drive transformers. Operation and waveforms are exactly those of a conventional half bridge.

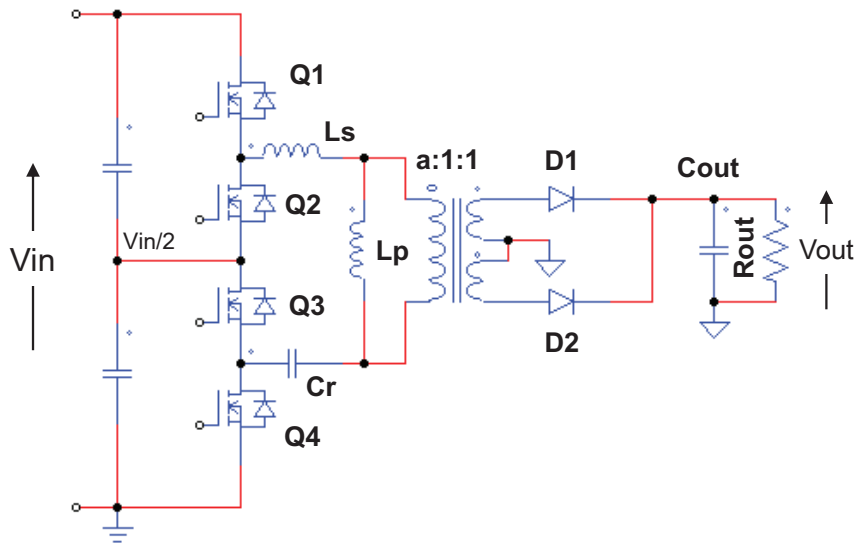


Figure 29.5: Three-level half bridge LLC converter.

A slightly different connection is considered in [76], which requires a slightly different driving scheme but the operation and the waveforms are essentially unchanged.

The multilevel approach, however, enables different driving schemes that may provide the converter with new properties. This is the case, for example, with the frequency doubling driving scheme proposed in [100], that is shown in the timing diagrams of Figure 29.6, along with the conventional driving scheme previously considered.

In this driving scheme, the pair Q1–Q4 is turned on with 25% duty cycle and the pair Q2–Q3 with 75% duty cycle, with the two PWM pulse trains displaced by 50% of switching period.

By doing so, the tank circuit is driven with half input voltage at a frequency double of that of the two PWM pulse trains. This is quite interesting because, according to the design objective, one can reduce the transformer size while keeping switching losses at a low level or keep the same transformer size and further reduce switching losses.

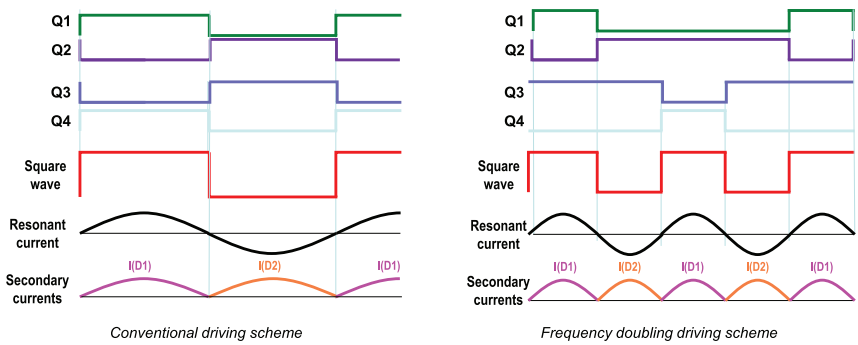


Figure 29.6: Two possible driving schemes for three-level half bridge LLC converter.

A drawback of this operation is the different current stress for the two pairs: the Q1–Q4 pair carries 1/4, and the Q2–Q3 pair 3/4 of total resonant current.

Finally, another good point to mention is that with both driving schemes there is an intrinsic input voltage self-balance mechanism so that the two stacked half bridges share the input voltage equally, which is a benign characteristic since it saves control overhead and increases converter reliability.

LLC Resonant Converter with Current Sink Output Filter

We have seen already that a weak point of the LLC converter is the large current stress on the output capacitor, so that it needs to be designed to withstand the ac component of the secondary current. We have also seen that one way to avoid this issue is to use the multiphase approach with interleaving, which however increases complexity and cost, so that it appears more justified at higher power levels.

In [45], [46] a modification of the LLC converter is proposed that uses a current sink output filter, i.e., adds an output inductor Lo between the rectifier block and the output capacitor as depicted in Figure 29.7. Instead, Figure 29.8 shows the typical key waveforms.

With this addition, the output capacitor can be significantly reduced, thus reducing also its size, weight and cost. It is therefore an interesting topology for high output current applications.

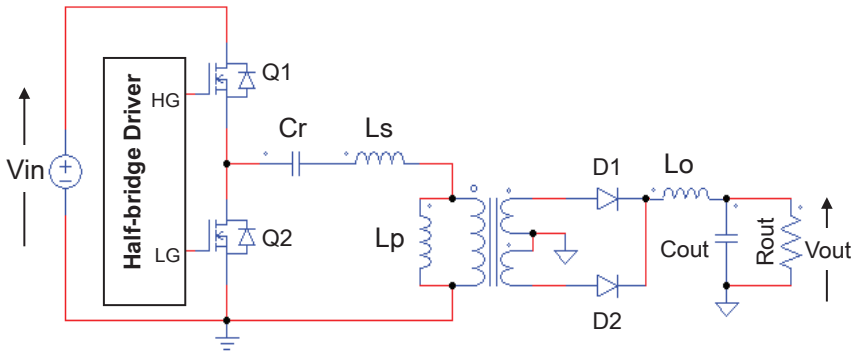
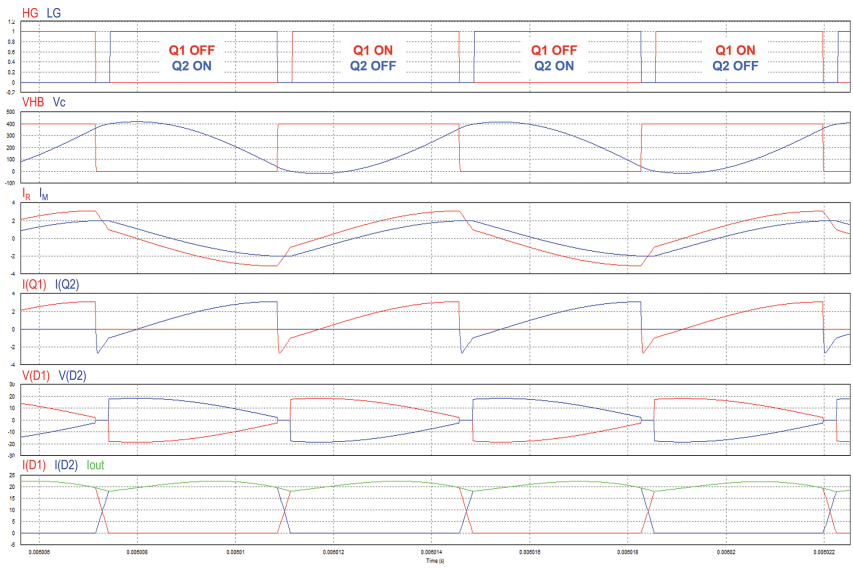


Figure 29.7: LLC resonant converter (half bridge) with current sink output filter.



HG= Q1 gate	VHB = Node HB voltage	I_R = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LG = Q2 gate	Vc = Resonant capacitor voltage	I_M = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

Figure 29.8: LLC resonant converter with current sink output filter: key waveforms.

Compared to the conventional LLC converter, the current sink output filter changes the operation of the converter completely.

The main resonant tank is composed of Lp and Cr and there is essentially a single resonance frequency. The converter can operate only

above resonance and, as visible in Figure 29.8, the tank current looks much like that of the conventional LLC converter when operated above resonance.

To a first-order approximation, neither *Ls* nor *Lo* participate to resonance. *Ls* just smooths the edges of the resonant current that follow the half bridge toggling, and in some cases may help achieve ZVS. Normally it can be substantially reduced, so that slotted bobbins might be unnecessary for magnetic integration. *Lo* can be regarded as a sort of current flywheel and in the analysis of the circuit can be replaced by a current source.

The switching frequency range is basically as narrow as with the traditional LLC. Rather, at light load is definitely narrower.

In fact, the output inductor cancels the effect of the parasitic capacitance of the secondary rectifiers because it blocks the initial "current spike" that occurs when one rectifier is going to be forward biased and that in the conventional LLC converter goes to the output. In this case, this current spike goes through the parasitic capacitance of the other rectifier. For this reason the switching frequency does not need to go that high to reduce the energy per cycle transferred by the normal mechanism. Needless to say, for the same reasons this topology is immune to the feedback reversal phenomenon at light load.

The adverse side effect of the output inductor *Lo* is that the reverse voltage applied to the secondary rectifiers increases significantly, 50% or even more than $2 \cdot Vout$, depending on the characteristics of the tank circuit.

Some additional insight on its operation can be given by its FHA analysis. Figure 29.9 shows the plot of the voltage gain $|M|$:

$$|M(x,Q)| = \frac{8}{\pi^2} \frac{x^2}{\sqrt{(x^2-1)^2 + Q^2 x^2}}, \tag{29.1}$$

where:

$$f_R = \frac{1}{2\pi\sqrt{Lp\,Cr}}; \quad Q = \frac{Z_0}{Re} = \frac{8}{\pi^2}\frac{Z_0}{a^2 Rout}; \quad Z_0 = \sqrt{\frac{Lp}{Cr}}. \tag{29.2}$$

All curves have an horizontal asymptote $M_\infty = 8/\pi^2$ when $x \to \infty$. This poses a constraint on α and, then, on the turn ratio a (reminder:

$\alpha = 2a$ in the half bridge and $\alpha = a$ in the full bridge); in the half bridge:

$$a > \frac{4}{\pi^2} \frac{Vin_{max}}{Vout}. \tag{29.3}$$

The curve with $Q = 0$ has a vertical asymptote when $x \to 1$. The inductive operating region will be that included between the curve $Q = 0$ and the curve $B_M(x)$ representing the capacitive mode borderline. A necessary condition for the converter to operate in the inductive region is to operate above resonance ($x > 1$).

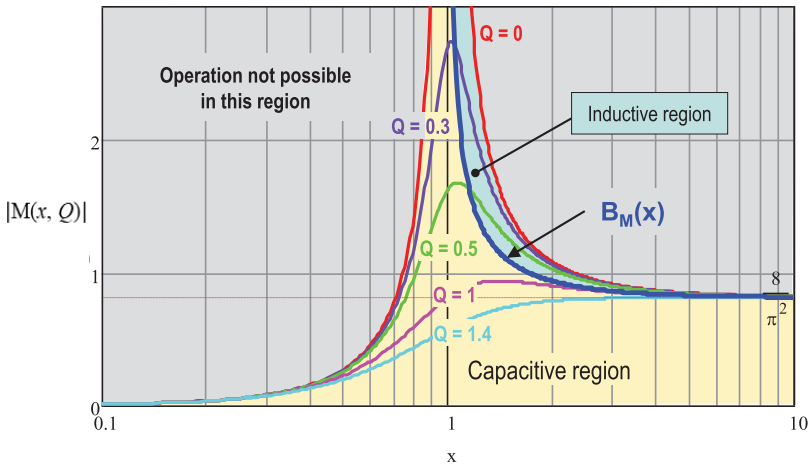


Figure 29.9: LLC resonant converter with current sink output filter: plot of $|M(x, Q)|$.

As visible in the key waveforms of Figure 29.8, the shape of the resonant current is piecewise sinusoidal and has significant harmonics. Therefore the quantitative results of an FHA-based analysis are not so accurate and a reliable design procedure should rather be based on a TDA analysis.

30

Single-Stage LLC PFC

The IEC 61000-3-2 regulation sets limits to the harmonic currents drawn by electrical equipment connected to public low-voltage distribution systems, with the objective of maintaining mains voltage quality. It is applicable to electrical and electronic equipment using voltage not less than 220 *Vac* and having a rated input current not exceeding 16 A per phase.

This regulation considers four classes of electronic equipment, the most important of which in this context are class C (lighting equipment with a rated input power in excess of 5 W) and Class D. The IEC 61000-3-2 specifies that class D equipment includes personal computers and personal computer monitors, television receivers, refrigerators and freezers with one or more variable-speed drives to control one or more compressor motors, with a rated input power included between 75 W and 600 W. De facto, all ICT equipment (e.g., ac–dc adapters for portable computers, large printers) with an input power over 75 W is considered as belonging to class D and then required to comply with the IEC 61000-3-2. Not only, quite often even power supplies of equipment not considered by the regulation are specified and built to comply with the class D limits (e.g. server and telecom SMPS).

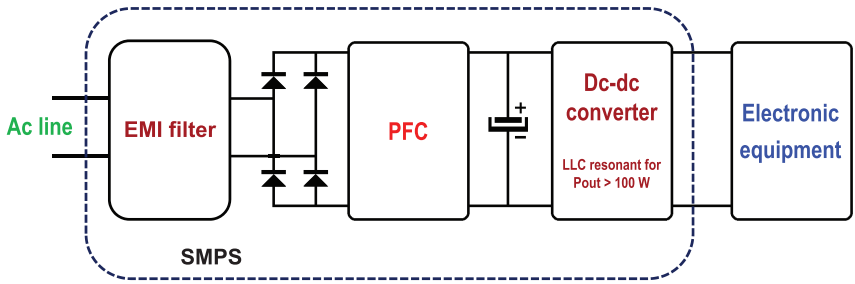


Figure 30.1: Typical two-stage architecture of a power factor corrected SMPS.

There are different solutions to address the compliance with the IEC 61000-3-2, but by far the most common in industry is the addition of an electronic front-end circuit, the so-called active power factor corrector (PFC). In its typical implementation, a PFC is a switch-mode converter directly supplied by the rectified mains, without any energy buffer capacitor after the bridge rectifier (the so-called bulk capacitor), and controlled so as to draw from the power line a sinusoidal current in phase with the voltage. This results in unity power factor, PF = 1.

As shown in Figure 30.1, a typical power-factor-corrected SMPS has a two-stage architecture: a PFC stage front-end (often called a PFC pre-regulator) and a cascaded dc–dc converter. The term pre-regulator stems from the fact that the PFC front-end normally provides a regulated output voltage to the cascaded dc–dc converter, whose design can then be optimized for a narrow input voltage range.

Usually, a PFC pre-regulator is realized with a boost converter, which is a non-isolated topology, so that the cascaded dc–dc converter is responsible for providing the safety isolation required in essentially all power supplies of class D equipment.

The boost converter can essentially cover the entire power range of class C and D equipment, whereas the cascaded dc-dc converter uses different topologies depending on the power level. Flyback converters are most used in the low power range, say up to 100 W, the LLC resonant converter has replaced other topologies at power levels over 100 W.

However, there are applications where having an isolated PFC cascaded by one or more non-isolated converters may be advantageous.

This is the case, for example, of multioutput SMPS or LED drivers, or the case of USB-PD compliant chargers for mobile equipment, single and multiport. Other applications (e.g., battery chargers) are tolerant to the low-frequency ripple of a PFC output and an isolated PFC might offer substantial cost saving by using a single-stage architecture.

Flyback-based isolated PFCs are a good choice up to 50–60 W (they are very often used in lighting equipment). For higher power levels there are solutions based on Cŭk or SEPIC converters. Unfortunately there is no simple and effective way to introduce isolation in the conventional boost converter. In this context, an isolated PFC based on the LLC resonant converter, i.e., a *Single-stage LLC PFC*, might be an attractive solution.

The question that arises is if the LLC converter can perform as a PFC stage when supplied from a rectified sinusoidal voltage that goes all the way from zero to the peak. When the instantaneous input voltage moves toward a zero-crossing, to regulate the output voltage the required voltage gain becomes larger and larger and tends to infinity when the instantaneous input voltage is zero. However, since the objective is to draw from the power line a current proportional to the line voltage, as the instantaneous input voltage moves toward a zero-crossing the load becomes lower and lower. As the FHA analysis has shown, the LLC converter has a much higher voltage gain at light load than at heavy load, and that it even goes to infinity at zero load ($Q = 0$) when the switching frequency equals the lower resonance frequency f_{R2}. Therefore, the LLC converter has the potential to work as a PFC stage.

FHA Analysis of LLC PFC

The FHA analysis of the LLC converter discussed in Part IV was developed based on the assumption that the converter was supplied by a dc input voltage (or, rather, by a substantially dc input voltage), and led to a series of design guidelines for the tank circuit.

The FHA approach can be extended to an LLC converter supplied by a rectified sinusoidal voltage at the line frequency f_{line} that goes all the way from zero to the peak. The underlying assumption is the so-called quasi-static approximation: the operating point changes with

the instantaneous phase angle θ of the rectified sinusoid slowly enough to consider the system always operating in steady-state conditions. This is justified by the line frequency f_{line} being much lower than the characteristic frequency associated to the response time of the converter.

As previously highlighted, since the output voltage will be regulated at a constant value, the required gain will not be constant but will vary along the instantaneous phase angle θ. If with Vin we denote the rms value of the line voltage, Eq. 19.1 can be rewritten as follows:

$$M_{req}\,(\,Vin, \theta) = \alpha \frac{Vout + V_{Rect}}{\sqrt{2}\;Vin \sin\theta}. \tag{30.1}$$

Its plot is shown in Figure 30.2. Furthermore, having $PF = 1$ implies that also the input and output power are not constant along θ. Irrespective of the topology, in a PFC stage, which can be regarded as a *resistor emulator*, the instantaneous input power swings all the way from 0 (at the zero-crossings of voltage and current) to twice the average power Pin (equal to $Pout/\eta$, where η is the efficiency) on the peaks of voltage and current, as inferable from (30.2) and shown in the plot of Figure 30.3:

$$Pin(\theta) = 2\;Vin\,Iin \sin^2\theta = 2Pin \sin^2\theta = 2\frac{Pout}{\eta}\sin^2\theta, \tag{30.2}$$

where Iin is the rms value of the line current. Reminding that the average power Pin can be expressed also as half the product of the peak line voltage $Vin_{pk} = \sqrt{2}Vin$ and peak line current $Iin_{pk} = \sqrt{2}Iin$, from (30.2) evaluated at $\theta = \pi/2$ we derive:

$$Pin = Vin_{pk} Iin_{pk}. \tag{30.3}$$

Therefore, on the peak of the sinusoidal line voltage the converter operates as if it was powered by a dc voltage equal to Vin_{pk}, drawing a dc current equal to Iin_{pk}. As a consequence, the first-harmonic representation of the input port can be described by the same equations seen for the dc case where Vin_{pk} replaces Vin in (13.2), (13.3) and (13.6), and Iin_{pk} replaces Iin in (13.5) and (13.6).

Also, the ac resistance (13.13) and the quality factor (13.23) vary along θ. Substituting (30.2) in (13.13) and (13.23) yields respectively:

$$Rout_{ac}(\theta) = \frac{4}{\pi^2}\frac{Vout^2}{Pout \sin^2\theta}\left(1 + \frac{V_{Rect}}{Vout}\right), \tag{30.4}$$

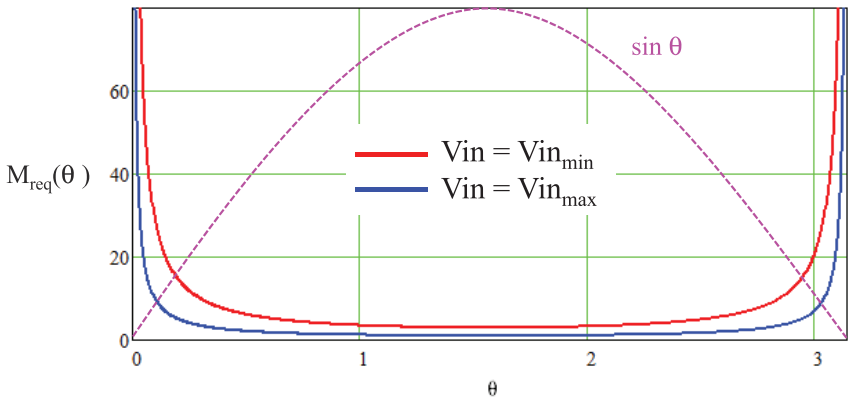


Figure 30.2: Minimum gain required for regulation in a single-stage PFC LLC.

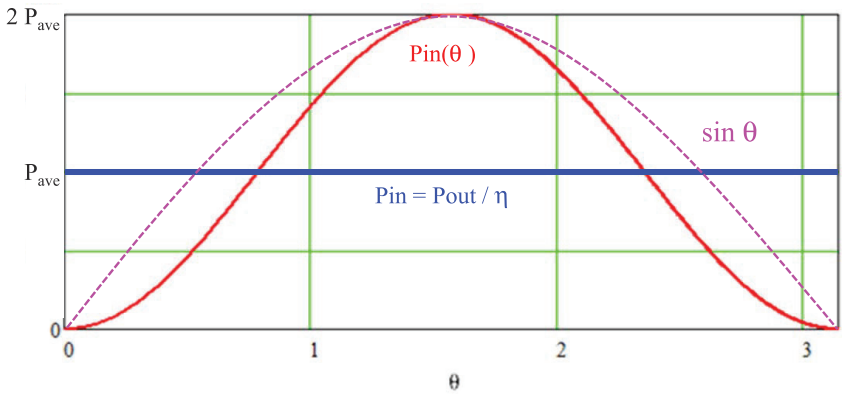


Figure 30.3: Instantaneous power and average (dc) power.

$$Q(\theta) = \frac{\pi^2}{4}\frac{Z_0}{a^2}\frac{Pout}{Vout^2}\frac{1}{1+\frac{V_{Rect}}{Vout}}\sin^2\theta = Q_0\sin^2\theta. \tag{30.5}$$

Finally, the voltage gain $|M|$ given by (15.2) will be a function of θ too:

$$|M(x,k,Q_0,\theta)| = \frac{1}{\sqrt{\left[1+\frac{1}{k}\left(1-\frac{1}{x^2}\right)\right]^2 + Q_0^2\sin^4\theta\left(x-\frac{1}{x}\right)^2}}. \tag{30.6}$$

Figure 30.4 shows the voltage gain $|M|$ vs. the normalized frequency, plotted at a fixed output level, with the phase angle θ as the parameter.

Three plots are provided at $\pi/2$, $\pi/3$, $\pi/4$ while the horizontal dashed lines are the required gains at the minimum input voltage (where the gain needs to be highest), with θ equal to $\pi/2$, $\pi/3$, $\pi/4$ respectively.

It is possible to see that at all these angles there is an intersection of the horizontal line with the corresponding $|M|$ curve that lies in the inductive region. This means that an operating point for the converter exists and that in this operating point the converter works with ZVS. This condition, however, should be verified for any angle θ included in $(0, \pi/2)$ to ensure that the output voltage can be regulated.

In [73] it is demonstrated that a sufficient condition for the converter to achieve regulation in all operating conditions is that voltage gain at $f_{sw} = f_{R2}$ and $\theta = \pi/2$ is larger than the required gain at the minimum

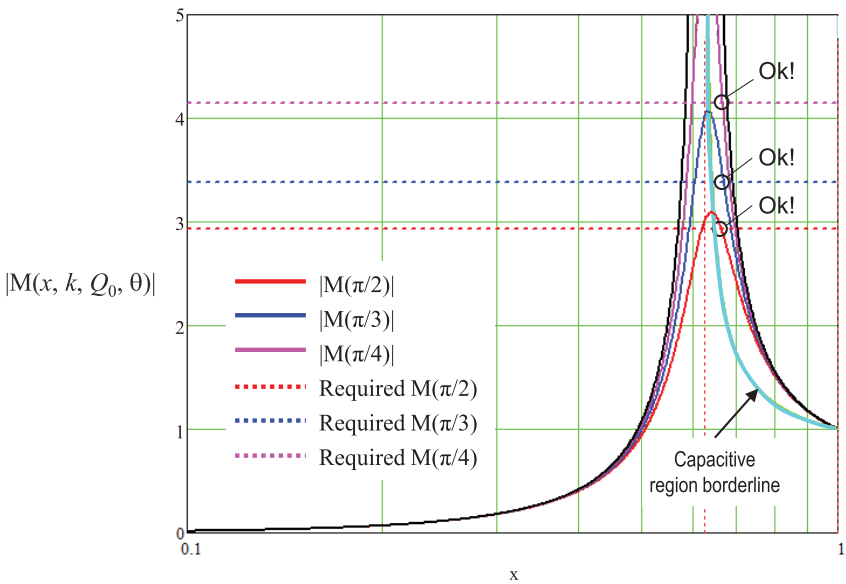


Figure 30.4: Voltage gain curves for different phase angles and comparison to the minimum required gain to achieve output voltage regulation.

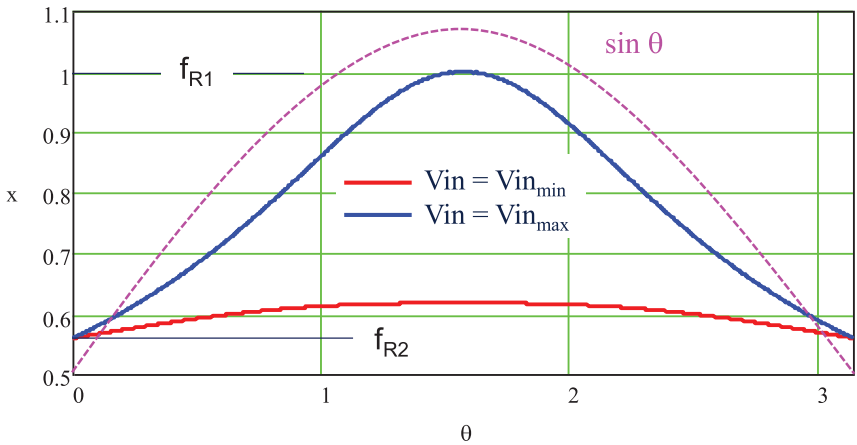


Figure 30.5: Normalized switching frequency vs. instantaneous phase angle.

input voltage and $\theta = \pi/2$:

$$\frac{1}{Q_0}\frac{\sqrt{1+k}}{k} > \alpha\frac{Vout}{\sqrt{2}\ Vin_{min}}. \tag{30.7}$$

This condition is a fundamental design constraint.

By equating the voltage gain $|M|$ (30.6) to the required gain (30.1) it is possible to find how the normalized switching frequency vary along the phase angle θ. This is illustrated in the plot of Figure 30.5.

The switching frequency peaks at $\theta = \pi/2$ and decreases as the instantaneous line voltage goes towards the zero-crossing, where it reaches the lower resonance frequency f_{R2}.

Design Considerations and Step-by-Step Design Procedure

Although with a single-stage LLC PFC it is possible to handle power levels well above 1 kW using the full bridge configuration [57], the majority of the target applications for such a single-stage LLC PFC stage are in the few hundred watts. Therefore, we will consider the half bridge configuration and it will be $\alpha = 2a$.

Table 30.1 lists a typical set of electrical specifications for a draft design of a single-stage LLC PFC converter. We will consider a procedure

Table 30.1: Reference electrical specification for a single-stage LLC PFC

Symbol	Name	Unit
$Vin_{min} - Vin_{max}$	Input voltage range (rms values)	Vac
$Vout$	Regulated output voltage	Vdc
$Pout_{min} - Pout_{max}$	Output power range	W
η	Estimated efficiency@$Pout_{max}$, Vin_{min}	%
f_{R1}	Upper resonance frequency	kHz
f_{R2}	Lower resonance frequency	kHz
C_{HB}	Half bridge midpoint estimated capacitance	pF
T_D	Dead-time	ns

based on them, tracing those outlined for the dc input voltage case in Part IV, Section 19, though based on a slightly different strategy:

(1) The converter will be designed to work in the below resonance region with the switching frequency ranging between the lower and the upper resonance frequencies. In terms of normalized frequency this means:

$$\frac{1}{\sqrt{1+k}} < x < 1. \tag{30.8}$$

There is not a predefined nominal input voltage where the converter may operate in optimal conditions. It seems that there is no special benefit in operating the converter above resonance, it just widens the frequency range.

(2) The converter will work at resonance ($M = 1$) at the maximum input voltage for $\theta = \pi/2$. This determines the transformer turns ratio (APR model):

$$a = \frac{\sqrt{2}}{2} \frac{Vin_{max}}{Vout + V_{Rect}}. \tag{30.9}$$

With this choice, reminding that in the half bridge, the required gain at minimum input voltage for $\theta = \pi/2$ is:

$$M_{req}\left(Vin_{min}, \frac{\pi}{2}\right) = 2a \frac{Vout + V_{Rect}}{\sqrt{2}\, Vin_{min}} = \frac{Vin_{max}}{Vin_{min}}. \tag{30.10}$$

(3) The converter must be able to regulate down to zero load at maximum input voltage.

(4) The quality factor Q_0 will be chosen so that converter will always work with ZVS, from zero load to Po_{max}. As also visible in Figure 30.4, the operating point closest to the capacitive region borderline is when the converter works with the minimum input voltage and full load, on the peak of the sinusoid ($\theta = \pi/2$). Choosing Q_0 so that ZVS and minimum gain conditions are both fulfilled, that will guarantee that the required voltage gain is always intercepted and that unity power factor ($PF = 1$) can be achieved while operating with ZVS.

The discussion presented so far can be summarized in a step-by-step design procedure based on the specification given in Table 30.1.

Step 1. Calculate a so that converter will work at resonance at maximum input voltage peak using (30.9).

Step 2. Calculate the output resistance Re:

$$Re = \frac{4}{\pi^2} a^2 \frac{Vout^2}{Pout_{max}} \left(1 + \frac{V_{Rect}}{Vout}\right). \tag{30.11}$$

Step 3. Calculate the maximum voltage gain M_{max} at $Vin = Vin_{min}$ and $\theta = \pi/2$ using (30.1).

$$M_{max} = 2a \frac{Vout + V_{Rect}}{\sqrt{2}\, Vin_{min}}. \tag{30.12}$$

Step 4. Calculate k so that the actual lower resonance frequency is f_{R2}:

$$k = \left(\frac{f_{R1}}{f_{R2}}\right)^2 - 1. \tag{30.13}$$

Step 5. Calculate the maximum Q_0 value, Q_{max1}, necessary to stay in the inductive region at minimum Vin and maximum load. From (15.7):

$$Q_{max1} = \frac{1}{k M_{max}} \sqrt{\frac{{M_{max}}^2}{{M_{max}}^2 - 1} + k}. \tag{30.14}$$

Step 6. Calculate the maximum Q_0 value, Q_{max2}, to ensure ZVS at zero load and maximum Vin. From (19.23), reminding that $x_{max} = 1$:

$$Q_{max2} = \frac{2}{\pi} \frac{1}{k} \frac{T_D}{Re\, C_{HB}}. \tag{30.15}$$

Step 7. Calculate the maximum Q_0 value, Q_{max3}, to ensure that the minimum gain requirement is fulfilled. From (30.7):

$$Q_{max3} = \frac{\sqrt{2}}{2}\frac{1}{a}\frac{\sqrt{1+k}}{k}\frac{Vin_{min}}{Vout + V_{Rect}}. \tag{30.16}$$

Step 8. Choose a value of Q_0, Q_S, such that $Q_S \leq min\ (Q_{max1}, Q_{max2}, Q_{max3})$.

Step 9. Calculate the normalized minimum operating frequency at $Vin = Vin_{min}$, $Pout = Pout_{max}$ and $\theta = \pi/2$, x_{min}, using (19.14) with $Q_B = Q_{max1}$:

$$x_{min} \cong \frac{1}{\sqrt{1 + k\left(1 - \frac{1}{1 + \left(\frac{Q_S}{Q_{max1}}\right)^5}\right)}}. \tag{30.17}$$

Step 10. Calculate the phase-shift φ_{min} of the tank current at $Vin = Vin_{min}$, $Pout = Pout_{max}$ and $\theta = \pi/2$ with (19.17) and check if the ZVS condition (19.27) is fulfilled. If so, proceed to step 11, otherwise choose a smaller value for Q_S and go back to Step 9.

Step 11. Calculate the characteristic impedance of the tank circuit and all component values with (19.10), reported here for the reader's convenience:

$$Z_0 = Re\ Q_S; \quad Cr = \frac{1}{2\pi f_{R1} Z_0}; \quad Ls = \frac{Z_0}{2\pi f_{R1}}; \quad Lp = k\,Ls. \tag{30.18}$$

Step 12. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer with (9.3), reported here for the reader's convenience:

$$n = a\sqrt{1 + \frac{Ls}{Lp}}; \quad L_\mu = \sqrt{LpL_1}; \quad L_{L1} = L_1 - L_\mu; \quad L_{L2} = \frac{L_{L1}}{n^2}. \tag{30.19}$$

Step 13. Calculate the maximum peak of the tank current to set up the overcurrent means by (19.15) where the dc value Vin becomes

$Vin_{pk} = \sqrt{2}\,Vin$, with Vin rms value of the line voltage:

$$I_{R1pk} = \begin{cases} \dfrac{\pi}{\sqrt{2}\eta}\dfrac{Pout_{max}}{Vin_{min}}\dfrac{1}{\cos\varphi_{min}} & \text{(HB)} \\ \dfrac{\pi}{2\sqrt{2}\eta}\dfrac{Pout_{max}}{Vin_{min}}\dfrac{1}{\cos\varphi_{min}} & \text{(FB)} \end{cases}. \tag{30.20}$$

To illustrate the just outlined design procedure, let us consider a fully developed example. Table 30.2 lists the electrical specification of an exemplary single-stage LLC-PFC intended to power an LED driver. Diode rectification will be used due to the high output voltage.

Table 30.2: Exemplary single-stage LLC PFC for LED driver: Electrical specification

Symbol	Name	Value	Unit
$Vin_{min} - Vin_{max}$	Input voltage range (rms values)	88–264	Vac
$Vout$	Regulated output voltage	60	Vdc
V_{Rect}	Secondary rectifier forward drop	0.5	Vdc
$Pout_{min} - Pout_{max}$	Output power range	0–120	W
η	Estimated efficiency@$Pout_{max}$, Vin_{min}	91	%
f_{R1}	Upper resonance frequency	200	kHz
f_{R2}	Lower resonance frequency	100	kHz
C_{HB}	Half bridge midpoint estimated capacitance	150	pF
T_D	Dead-time	300	ns
Cp	Secondary-side parasitic capacitance (est.)	2	nF

Step 1. Calculate a so that converter will work at resonance at maximum input voltage peak:

$$a = \frac{\sqrt{2}}{2}\frac{Vin_{max}}{Vout + V_{Rect}} = \frac{\sqrt{2}}{2}\frac{264}{60 + 0.5} = 3.086.$$

Step 2. Calculate the output resistance Re:

$$Re = \frac{4}{\pi^2}a^2\frac{Vout^2}{Pout_{max}}\left(1 + \frac{V_{Rect}}{Vout}\right) = \frac{4}{\pi^2}3.086^2\frac{60^2}{120}\left(1 + \frac{0.5}{60}\right) = 116.8\,\Omega.$$

Step 3. Calculate the maximum voltage gain M_{max}:

$$M_{max} = 2a\frac{Vout + V_{Rect}}{\sqrt{2}\,Vin_{min}} = 23.086\frac{60 + 0.5}{\sqrt{2}\cdot 88} = 3.$$

Step 4. Calculate k so that the actual lower resonance frequency is f_{R2}:

$$k = \left(\frac{f_{R1}}{f_{R2}}\right)^2 - 1 = (2)^2 - 1 = 3.$$

Step 5. Calculate the maximum Q_0 value, Q_{max1}, necessary to stay in the inductive region at minimum *Vin* and maximum load:

$$Q_{max1} = \frac{1}{kM_{max}}\sqrt{\frac{{M_{max}}^2}{{M_{max}}^2 - 1} + k} = \frac{1}{3 \cdot 3}\sqrt{\frac{3^2}{3^2 - 1} + 3} = 0.226.$$

Step 6. Calculate the maximum Q_0 value, Q_{max2}, to ensure ZVS at zero load and maximum *Vin*:

$$Q_{max2} = \frac{2}{\pi}\frac{1}{k}\frac{T_D}{Re\, C_{HB}} = \frac{2}{\pi}\frac{1}{3}\frac{300 \cdot 10^{-9}}{116.8 \cdot 150 \cdot 10^{-12}} = 3.634.$$

Step 7. Calculate the maximum Q_0 value, Q_{max3}, to ensure that the minimum gain requirement is fulfilled:

$$Q_{max3} = \frac{\sqrt{2}}{2}\frac{1}{a}\frac{\sqrt{1+k}}{k}\frac{Vin_{min}}{Vout + V_{Rect}} = \\ = \frac{\sqrt{2}}{2}\frac{1}{3.086}\frac{\sqrt{1+3}}{3}\frac{88}{60 + 0.5} = 0.222.$$

Step 8. Choose a value of Q_0, Q_S, such that $Q_S \leq min\ (Q_{max1}, Q_{max2}, Q_{max3})$:

$$Q_S = 0.2.$$

Step 9. Calculate the normalized minimum operating frequency at $Vin = Vin_{min}$, $Pout = Pout_{max}$ and $\theta = \pi/2$, x_{min}:

$$x_{min} \cong \frac{1}{\sqrt{1 + k\left(1 - \frac{1}{M_{max}^{1+\left(\frac{Q_S}{Q_{max1}}\right)^5}}\right)}} = \\ = \frac{1}{\sqrt{1 + 3\left(1 - \frac{1}{3^{1+\left(\frac{0.2}{0.226}\right)^5}}\right)}} = 0.538.$$

Step 10. Calculate the phase-shift φ_{min} of the tank current at $Vin = Vin_{min}$, $Pout = Pout_{max}$ and $\theta = \pi/2$, and check if ZVS condition

(18.18) is fulfilled:

$$\varphi_{min} = \tan^{-1} \frac{\left[1 + k + Q_S^2 k^2 \left(x_{min}^2 - 1\right)\right] x_{min}^2 - 1}{Q_S k^2 x_{min}^3} =$$

$$= \tan^{-1} \frac{\left[1 + 3 + 0.2^2 \cdot 3^2 \left(0.538^2 - 1\right)\right] 0.538^2 - 1}{0.2 \cdot 3^2 \cdot 0.538^3} = 0.29 \,\text{rad};$$

$$\frac{\varphi_{min}}{2\pi f_{R1}} \frac{1}{x_{min}} = \frac{0.29}{2\pi \cdot 200 \cdot 10^3} \frac{1}{0.538} = 429 \cdot 10^{-9} \,\text{s} > T_D = 250 \cdot 10^{-9} \,\text{s}.$$

Step 11. Calculate the characteristic impedance of the tank circuit and all component values:

$$Z_0 = Re\, Q_S = 116.8 \cdot 0.2 = 23.36 \,\Omega;$$

$$Cr = \frac{1}{2\pi f_{R1} Z_0} = \frac{1}{2\pi \cdot 200 \cdot 10^3 \cdot 23.36} = 34.1 \,\text{nF};$$

$$Ls = \frac{Z_0}{2\pi f_{R1}} \frac{23.36}{2\pi \cdot 200 \cdot 10^3} = 18.6 \;\mu\text{H};$$

$$Lp = k\; Ls = 3 \cdot 18.6 \cdot 10^{-6} = 55.8 \;\mu\text{H}.$$

Step 12. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer:

$$n = a\sqrt{1 + \frac{Ls}{Lp}} = 3.086\sqrt{1 + \frac{18.6}{55.8}} = 3.563;$$

$$L_\mu = \sqrt{Lp L_1} = \sqrt{55.8\,(55.8 + 18.6)} = 64.4 \;\; \mu\text{H};$$

$$L_{L1} = L_1 - L_\mu = 55.8 + 18.6 - 64.4 = 10 \;\; \mu\text{H};$$

$$L_{L2} = \frac{L_{L1}}{n^2} = \frac{10}{3.563^2} = 0.788 \;\mu\text{H}.$$

Step 13. Calculate the maximum peak of the tank current to set up the overcurrent means:

$$I_{R1pk} = \frac{\pi}{\sqrt{2}\eta} \frac{Pout_{max}}{Vin_{min}} \frac{1}{\cos\varphi_{min}} = \frac{\pi}{\sqrt{2} \cdot 0.91} \frac{120}{88} \frac{1}{\cos 0.29} = 3.473 \;\text{A}.$$

- Post-design checks:

  (a) Let us calculate the value of $\Gamma = Cp/Cr$ to assess the effect of Cp:

  $$\Gamma = \frac{Cp}{a^2 Cr} = \frac{2 \cdot 10^{-9}}{3.086^2 \cdot 34.1 \cdot 10^{-9}} = 0.012.$$

  The normalized frequency where no-load gain reverses is:

  $$x_V = \sqrt[4]{\frac{1}{k\Gamma}} = \sqrt[4]{\frac{1}{30.012}} = 2.29 > x_{max} = 2.$$

  Therefore the initial assumption of considering negligible the effect of Cp in this design is correct.

  (b) The ZVS condition check $Vin = Vin_{min}$, $Pout = Pout_{max}$ has been done based on condition (8.7). According to the algorithm described in Part II, Section 8, we need to check if (8.7) is applicable. Let us calculate the value of the switched current in those conditions:

  $$|I_{R0}| = I_{R1pk_{max}} \sin \varphi_{min} = 3.473 \cdot \sin 0.29 = 0.993 \text{ A}.$$

  The critical value provided by (8.9), adapted to the ac input case, is:

  $$I_{R0_{crit}} = \sqrt{2\frac{C_{HB}}{Ls}}\, Vin_{min} = \sqrt{2\frac{150 \cdot 10^{-12}}{18.6 \cdot 10^{-6}}}88 = 0.353 \text{ A}.$$

$|I_{R0}|$ is more than twice larger than the critical value, then (8.7) is acceptable.

Single-Stage LLC PFC Control Strategy

Among the available control techniques for resonant converters, average current mode control (ACMC) is the most suitable. DFC control, though not limiting the dynamic behavior of such a system (it is worth reminding that a PFC stage is a narrow bandwidth system, typically <20 Hz), is not applicable: the frequency profile in a line half-cycle is a too complex function of the input voltage, the output load and the instantaneous phase angle θ to be programmed directly.

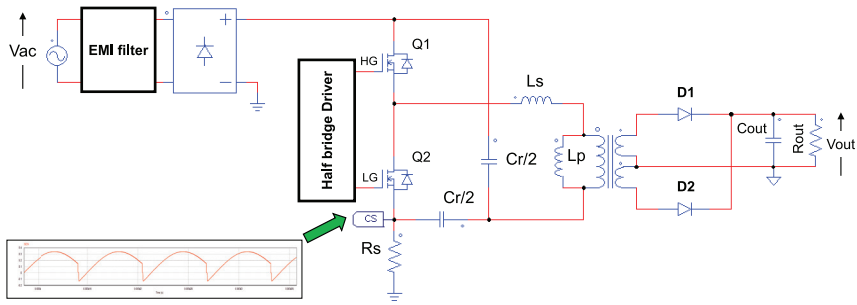


Figure 30.6: Single-stage LLC-PFC: power circuit reference schematic.

To conveniently apply ACMC to the half bridge single-stage LLC PFC, it is necessary to properly configure the power circuit. The suggested configuration is that with split resonant capacitors shown in Figure 30.6 and already discussed in Part II, Section 4. Notice how the sense resistor is connected, which allows the tank current to flow in the sense resistor Rs during both half cycles with the same (positive) sign. This makes the extraction of the average input current much easier and cleaner: a sense resistor in series to the tank circuit would result in zero average current, while sensing the input current only in the half-cycle where the high-side switch is on would result in an asymmetrical tank current.

ACMC is based on two nested loops: the inner current loop and the outer voltage loop, like in fixed-frequency CCM-operated boost PFC converters. The purpose of the current loop is to make the average input current closely track a sinusoidal reference, typically obtained from the rectified input voltage and properly adjusted in amplitude. The purpose of the voltage loop is to regulate the output voltage by properly setting the amplitude of the sinusoidal reference for the inner current loop. This structure is shown in the block diagram of Figure 30.7.

The output of the multiplier provides the current sense reference voltage V_{CSref}, by multiplying the feedback voltage V_{FB} coming from the voltage loop by a scaled down rectified input voltage to program the sinusoidal shape for the input current.

The VFF (voltage feedforward) block makes the feedback voltage V_{FB} dependent only on the output power level, eliminating the dependence on the input voltage.

The OPA, configured as an integrator, compares the current sense reference to the averaged voltage across the sense resistor Rs, connected as shown in Figure 30.6. The output of the OPA is the control voltage of the VCO that determines the switching frequency of the converter. Finally, the driver logic block drives the MOSFETs of the half bridge.

The outer loop can be based on a traditional TL431 + optocoupler arrangement like that shown in Figure 24.11. In fact, ACMC makes type-2 amplifier viable.

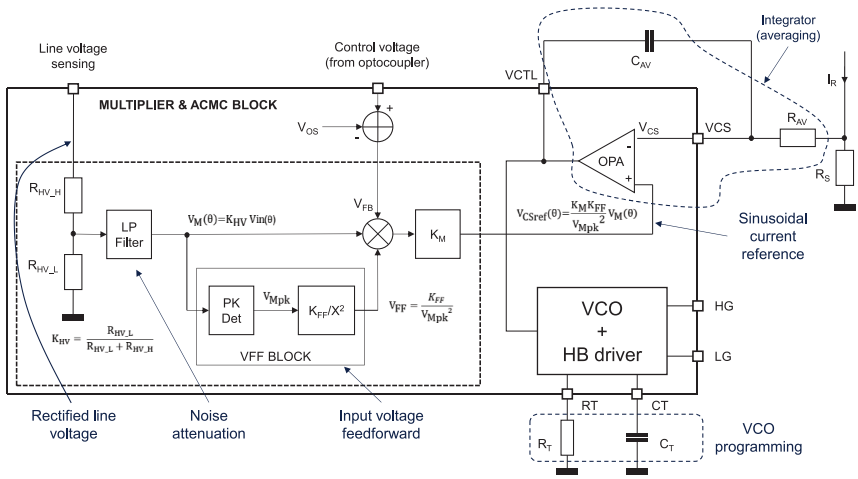


Figure 30.7: Single-stage LLC PFC: ACMC control loop block diagram.

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Dedicated to Anna and Alberto

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