Welcome to the World of Single-Slope Column-Level Analog-to-Digital Converters for CMOS Image Sensors

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ABSTRACT

This monograph introduces the reader into basic and advanced aspects of single-slope analog-to-digital converters (SS-ADC) applied in solid-state image sensors. It is based upon the developments that took place over the last three decades in this field. Already in the very early days of CMOS image sensors (CIS), the very first SS-ADC was implemented. The architecture of the SS-ADC is an appealing concept for column-level ADCs in a CIS. Especially the small silicon area occupied by the ADC and the low power consumption are very attractive features. Unfortunately the SS-ADC, as it originally was developed, is relatively slow. This monograph describes all advantages and limitations of the SS-ADC, as well as the various improvements mainly focusing on increasing the conversion speed. On academic as well as on industrial level various optimizations were proposed to make the devices not only faster, but also to increase their performance in terms of noise. Implementation of a digital

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correlated sampling technique or the application of multiple correlated sampling (without any hardware change) are a couple of examples how SS-ADCs contribute to improved image quality of the CIS.

Before diving into various architectures of a SS-ADC, the monograph starts with an overview of some basic building blocks of a CIS. Conceptual improvements are described, finally coming to the so-called "counting SS-ADC". A relatively large section is devoted to the theoretical analysis of the latter architecture, because this device has a unique combination of speed and low noise, two critical performance parameters for a CMOS image sensor.

1

Introduction

CMOS image sensors (CIS) have come a long way from the late 1980s and early 1990s up to where they are today. However, already since the very first developments in the field, column-level single-slope analog-to-digital converters (SS-ADC) were incorporated [7]. The combination of an image sensor with on-chip column-level ADCs demonstrates exceptional performance as far as speed and power are concerned. It is not only the imaging array that went through a lot of new developments, so did the SS-ADC configuration. This monograph gives an overview and background of the various developments of the SS-ADCs.

In Section 2 of this monograph, some background information is given about the general CIS architecture, the CIS pixels and the noise sources present in a CIS. Part of this general technical information is used in the remaining section of the monograph. Section 3 describes the various architectures used in a SS-ADC, starting with the most simple and earliest device described to the more complex architectures that include additional features in the ADC. After the description of the overall structure of the SS-ADCs, in Section 4 more details are studied about the various building blocks that are used in the SS-ADCs, such as amplifiers, comparators, ramp generators and counters. The monograph concludes with a future outlook, included in Section 5.

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