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Systematic Design of Analog CMOS Circuits with Lookup Tables

Paul G. A. Jespers
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Systematic Design of Analog CMOS Circuits with Lookup Tables

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ABSTRACT

The idea underlying the methodology described in this monograph consists in the use of a set of Lookup Tables embodying device data extracted prior from systematic runs done once and for all using an advanced circuit simulator, the same as used for final design verifications. In this way, all parameters put to use during the sizing procedure incorporate not only the bearings of bias conditions and geometry, but also every second-order effect present in the simulator's model, in particular short-channel effects. Consequently, the number of verification simulations one has to perform is not only substantially reduced, but the designer may concentrate on actual design strategies without being bothered by inconsistencies caused by poor models or inappropriate parameters.

*The author acknowledges the kind support of Prof. Boris Murmann in writing this monograph.

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1

General Philosophy of the Design Methodology

1.1 The Objective

Mainstream textbooks explain how electronic circuits work, but cover very little on how to conceive them. In this monograph, which elaborates further beyond [5], we aim to give an answer to the question of how to determine currents, channel lengths and widths of CMOS circuits, so as to optimally satisfy design specifications.

The usual way of doing this is to run a series of simulations interspersed with corrective tune-ups (see Figure 1.1). To start with, the designer determines plausible transistor sizes and currents supposed to meet the target objectives. To this effect, he/she carries out prospective "hand calculations, that take advantage of elementary transistor models to avoid cumbersome developments. The quadratic model, for instance, is a plausible candidate. Regrettably, the model's inability to render second-order effects such as DIBL and so on introduces inconsistencies that are augmented by the unavailability of parameters matching the final fab line. Not surprisingly, the outcome of any first simulation run may deviate substantially from the expected objectives. The designer consequently needs to amend the transistors sizes and currents, hoping to get closer to the desired goals. This is indicated by the dotted line

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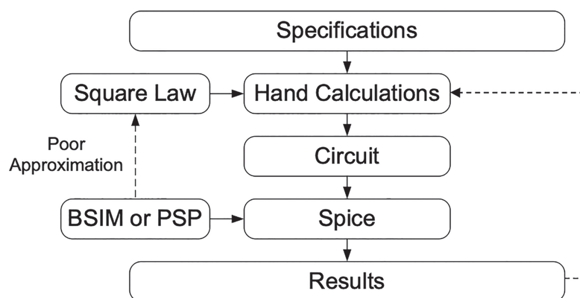

Figure 1.1: Traditional flow of sizing CMOS circuits iteratively.

that goes from results to hand calculations in Figure 1.1. He/she runs new simulations to check the adequacy of the changes made. Usually, not one but several cycles are needed to achieve the final design goal. At this point, the estimate of transistor sizes and currents is considered to be satisfactory. However, the result may be inadequate owing to the existence of eventual sub-optimal minima. Moreover, the design intent is lost, undocumented and difficult to re-use.

The intent of this monograph is to present a design methodology that replaces the iterative procedure of Figure 1.1 by a straightforward design approach that is illustrated in Figure 1.2. The method uses Lookup Tables (LUTs) instead of compact MOSFET models. Every Lookup Table defines a single parameter, specifically its dependence on bias and geometry. The data have been derived beforehand from simulations with advanced device models, the same as those put to use throughout

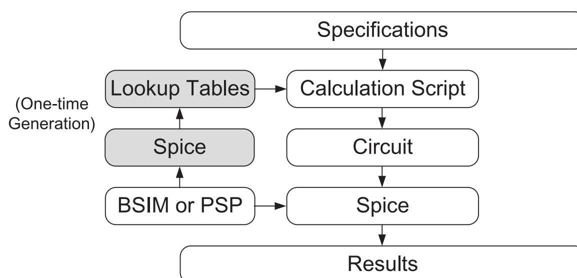

Figure 1.2: Flow of sizing CMOS circuits with pre-computed Lookup Tables [5].

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later SPICE simulations. Every parameter thus reflects the impact not only of bias and geometry but also of every effect the simulator handles (short-channel effects, DIBL, etc.). Since the designer is not bothered by misleading interpretations due to improper parameters or poor models, he/she can analyze and improve his calculation script without the need to run unnecessary SPICE simulations. He/she can evaluate the impact of forecasts induced by analytical expressions like those found in textbooks and resort to optimization following the modifications he/she introduces.

The tables we use in this monograph are derived for an example technology model, the 65-nm PSP model, considered in [5]. The tables report primarily small- and large-signal parameters at room temperature. Setting up such Lookup Tables is a task one has to undertake only once as long as the technology does not change. For the generation of such Lookup Tables, we invite the reader to Appendix 2 of [5]. Readers who want to get familiar with the Lookup Tables and the way to use the lookup Matlab functions described below, are invited to consult the G_m/I_D Starter Kit at http://web.stanford.edu/~murmann/gmid.html.

To the question of up to what channel lengths the above method applies, the answer is simple: the limit is that of the SPICE simulator used. As long as the SPICE models do not turn out to be wrong, the method is valid. We find proof of this in recent publications that make use of the methodology: [10] uses a 16-nm technology, while [8] presents a g_m/I_D design using the latest kinds of transistors [8].

1.2 Exemplary Lookup Tables

The tables used, which are consistent with the flow of Figure 1.2, are categorized into two classes: (1) the first class collects magnitudes of small- and large-signal parameters currently associated to the Quasi Static Model (QSM); (2) the second class concerns ratios of parameters that belong to the first class. Eventually, we may consider more sets of tables if other parameters like temperature or/and the impact of mismatch (e.g., slow/hot or fast/cold Lookup Tables) matter.

The conductance g_m, the output conductance g_{ds}, the input capacitance C_{gg} and the drain current I_D are typical parameters belonging

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to the Lookup Tables of the first class. Every parameter is categorized with respect to well-defined bias conditions and sizes. For what concerns the bias, each parameter is defined with respect to the applied voltages, the gate-to-source voltage V_{GS}, the drain-to-source voltage V_{DS}, and the source-to-substrate voltage V_{SB}. For what concerns the sizes, a range of gate lengths L is defined contrarily to the gate width W, which is assumed to have a fixed value. The reason is that since the vast majority of analog CMOS circuits take advantage of wide transistors, proportionality holds as far as W is concerned, an assumption that is reinforced when we take advantage of layout rules that help reduce the impact of border effects, as we will see further.

Proportionality leads us to the second class of Lookup Tables. These concern ratios of parameters that belong to the first class. Typical examples are the drain current density J_D equal to I_D/W, the intrinsic low-frequency gain of the common-source transistor g_m/g_{ds}, the transit frequency g_m/C_{gg} and the transconductance efficiency g_m/I_D. Since the numerator and the denominator of every ratio are assumed to vary proportionally to the width, any parameter that belongs to the second class is assumed to be a width-independent quantity.

1.2.1 Class-1 Lookup Tables

Let us consider an example of a class-1 Lookup Table parameter. The Matlab instruction below defines the drain current I_D of the common-source transistor:

$$I_D = \text{lookup}(\text{nch}, \textbf{`ID'}, \textbf{`VGS'}, \ldots, \textbf{`VDS'}, \ldots, \textbf{`VSB'}, \ldots, \textbf{`L'}, \ldots) \tag{1.1}$$

The output variable we are looking for is the drain current, **ID**. All other variables are input variables. The first one, nch, designates the type of transistor that we consider ($n$ch for n-channel or pch for p-channel). The remaining variables specify the terminal voltages of the transistor, V_{GS}, V_{DS} and V_{SB} [in V], and the gate length L [in μm]. The gate width is constant and chosen to be equal to 10 μm, in line with the assumption mentioned earlier. The input variables can be either scalars, vectors or matrices, the dimensions of the output variable adjusting automatically.

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Consider for instance a drain-to-source voltage V_{DS} equal to 0.6 V (half the supply voltage V_{DD} of 1.2 V), and a gate-to-source voltage V_{GS} swept from 0.3 to 0.7 V in steps of 0.1 V wide. We consider two gate lengths, 100 and 500 nm, respectively. The drain current expression boils down to the expression below, where the drain-to-source and source-to-bulk voltages are ignored, as both coincide with the consistent default values of the Lookup Tables, 0.6 and 0.0 V, respectively.

$$I_D = \text{lookup}(\text{nch}, \textbf{`ID'}, \textbf{`VGS'}, V_{GS}, \textbf{`L'}, L) \tag{1.2}$$

where:

$$V_{GS} = 0.3 : 0.1 : 0.7;$$
$$L = [0.1 \quad 0.5]:$$

What we get is the 2-by-5 matrix reproduced below that lists the drain current I_D versus V_{GS} from 0.3 V to 0.7 V horizontally and versus L from 0.1 to 0.5 μm vertically. The data illustrated by means of circles in the plot of Figure 1.3 represent the subsequent currents.

$$I_D(\text{mA}) = \begin{matrix} 0.0009 & 0.0142 & 0.0952 & 0.3130 & 0.6997 \\ 0.0003 & 0.0045 & 0.0278 & 0.0876 & 0.1939 \end{matrix} \tag{1.3}$$

Now, assume that we increase the width of the transistor from 10 to 20 μm. According to the assumption made earlier, the current doubles. Does this mean that we knowingly ignore edge effects? The answer is more specific. As mentioned before, most CMOS circuits take advantage of wide transistors. To support the premise, we reinforce proportionality by turning the layout of any transistor of arbitrary width W into a structure similar to the 10-μm-wide reference transistor shared by all Lookup Tables, as shown in Figure 1.4. The latter consists of 5 sub-transistors in parallel, each 2 μm wide. To implement a transistor of arbitrary width W, we divide the new device into an integer number of parallel sub-transistors whose common widths are as close as possible to the width of the reference sub-transistor. In this way, only small disparities differentiate the new from the reference sub-devices. In Figure 1.5, which is extracted from Appendix 3 of [5], we indeed see that, as soon as W exceeds 2 μm, the relative error affecting the current

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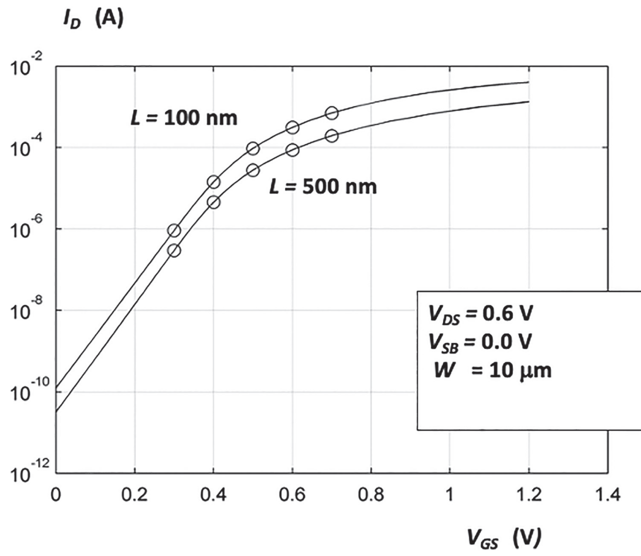

Figure 1.3: I_D versus V_{GS} data derived from (1.2).

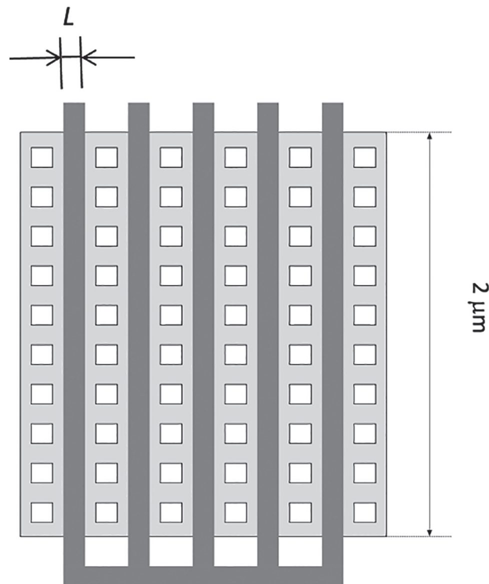

Figure 1.4: Layout of the reference transistor.

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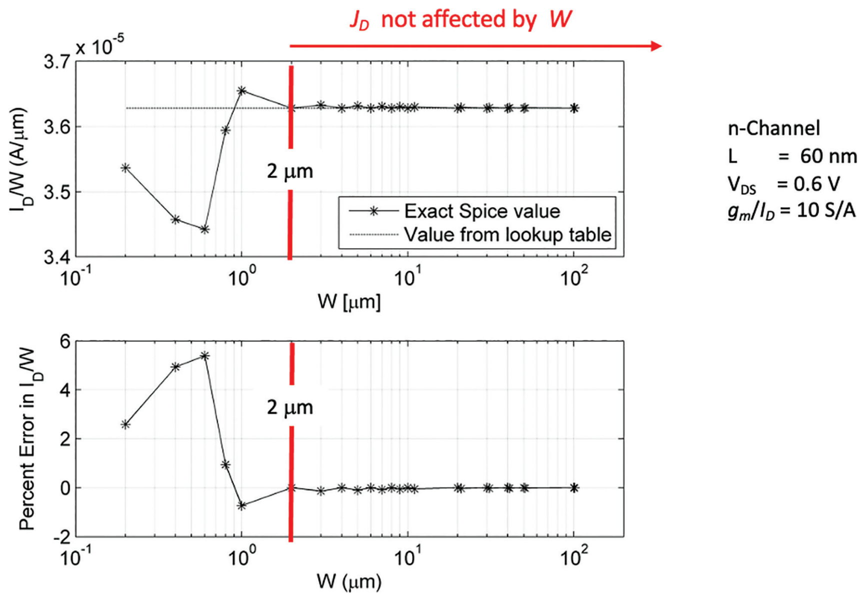

Figure 1.5: Convergence map of the drain current versus the width (reproduced by courtesy of C.U.P. [5]).

with respect to the real data becomes negligible. Proportionality is a key feature of the methodology and is exploited systematically throughout the remainder.

1.2.2 Class-2 Lookup Tables

Recall that the difference with respect to class-1 parameters is that all class-2 parameters are ratios of parameters that belong to class 1. Therefore, class-2 parameters are assumed to be width-independent quantities. Let us consider two examples: the drain current density J_D (**ID_W**) and the intrinsic gain g_m/g_{ds} (**GM_GDS**). We consider an open-drain common-source n-channel transistor; we assume that L varies from 0.1 to 0.4 μm in steps of 0.1 μm wide; and we take for V_{GS}, V_{DS} and V_{SB} the default values of the Tables, i.e., we consider the full range of gate-to-source voltages V_{GS} from 0 to 1.2 V and we assume for V_{DS} and V_{SB} 0.6 and 0.0 V, respectively. To assess J_D and A_{vo}, we consider the expressions below that make use of the same formalism as

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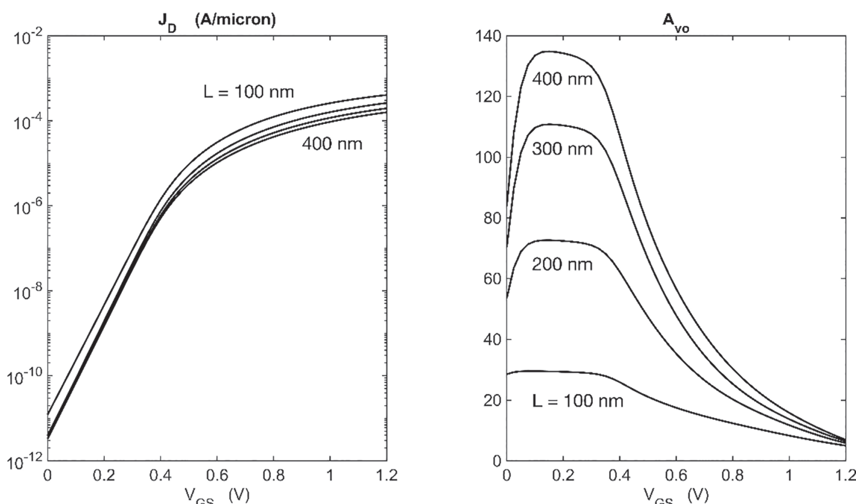

Figure 1.6: Drain current density J_D and open-drain low-frequency gain A_{VO} of the common-source stage versus V_{GS} for four different gate lengths.

for the class-1 parameters. We obtain the values for the drain current density J_D and the low-frequency gain A_{vo} shown in Figure 1.6. The first plot recalls Figure 1.3. The second plot illustrates the impact of V_{GS} and L on the gain.

$$J_D = \text{lookup}(\text{nch}, \textbf{`ID_W'}, \textbf{`L'}, \text{L}); \tag{1.4}$$

$$A_{vo} = \text{lookup}(\text{nch}, \textbf{`GM_GDS'}, \textbf{`L'}, \text{L}); \tag{1.5}$$

Among all class-2 parameters, two deserve special attention: the **transconductance efficiency** g_m/I_D (**GM_ID**) and the **transit frequency** g_m/C_{gg} (**GM_CGG**). These play an important role regarding the sizing of CMOS analog circuits, as we will see in the remaining.

The Transconductance Efficiency g_m/I_D

The transconductance efficiency g_m/I_D merges a small-signal parameter, the transconductance g_m, and a large-signal variable, the drain current I_D. The dimensions of the transconductance efficiency are V^{-1} but we opt for S/A, the latter being more illustrative of the significance of g_m/I_D.

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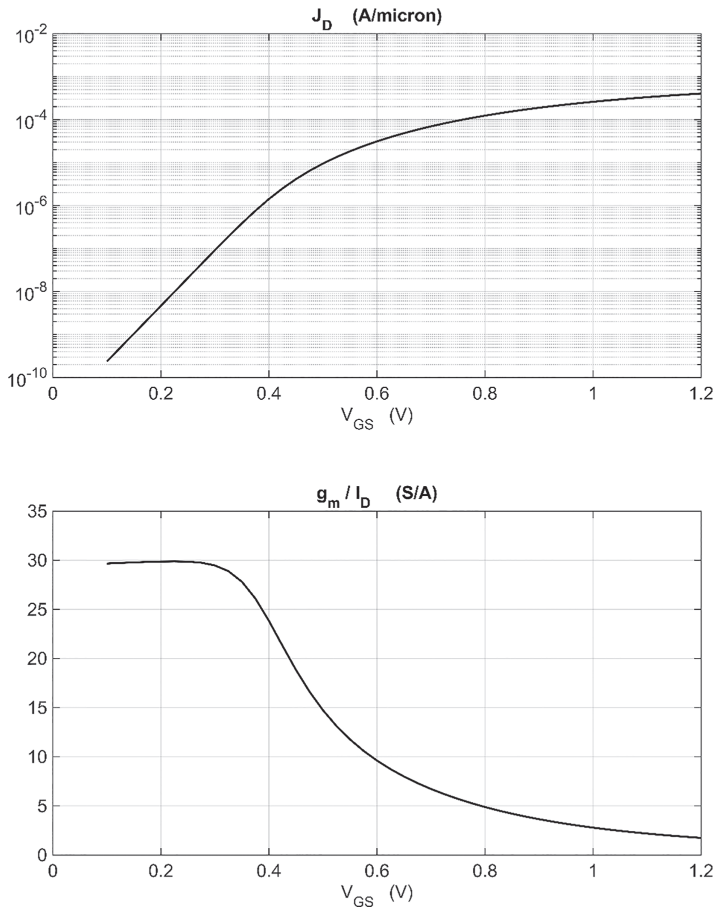

Figure 1.7: Drain current density J_D and transconductance efficiency g_m/I_D versus the gate-to-source voltage.

The use of g_m/I_D in order to fix the dimensions and currents of CMOS circuits has been introduced in a paper published in 1996 by Silveira *et al.* [7] and in [4]. We discuss the deeper meaning of this ratio hereafter.

To begin with, we plot g_m/I_D versus the gate-to-source voltage V_{GS} in Figure 1.7. The result that we obtain is easy to forecast since:

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_{GS}} = \frac{d\log(I_D)}{dV_{GS}} \tag{1.6}$$

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In other words, the graph representing g_m/I_D versus V_{GS} is nothing but a replica of the slope of the drain current when plotted in semi-log axes. This is confirmed in Figure 1.7, where we see above the semi-log plot versus V_{GS} of the drain current density J_D of the common-source MOS transistor according to (1.4), and, plotted in linear axes below, the transconductance efficiency g_m/I_D of the same transistor as per (1.7):

$$g_m/I_D = \text{lookup}(\text{nch}, \textbf{'GM_ID'}, \textbf{'L'}, \text{L}); \tag{1.7}$$

The lower curve is clearly the derivative of the upper curve. Whether we consider large- or short-channel devices, bulk or SOI technologies, 2-D or 3-D MOS transistors, the appearance of I_D and g_m/I_D does not alter practically. Two clear-cut sections are discernable in each characteristic. In the upper plot, as long as the gate-to-source voltage stays below 0.3 V, the drain current grows exponentially. Beyond, the growth rate starts to slow down. Likewise, the transconductance efficiency in the lower plot is the largest and almost constant as long as V_{GS} does not exceed 0.3 V. Beyond, the slope decreases continuously. These changes transcribe discrete physical phenomena that take place in the inversion layer of any transistor. When the gate voltage is low, the flow of mobile carriers from source to drain is mainly controlled by diffusion, while, as the current increases, the growing electrical field along the channel adds on drift current. At low level, the mechanism controlling the flow of mobile carriers is the same as in the neutral part of the base of bipolar transistors. With MOS transistors, however, the nature of the current changes as the gate voltage increases. Drift current is adding progressively to the diffusion current, turning the exponential growth of the drain current into a quadratic one. Weak-inversion conditions prevail when diffusion current dominates; strong-inversion conditions prevail when drift current dominates.

For a thorough analysis explaining the mechanisms controlling the changing nature of the drain current, please consult sources describing the "Charge Sheet Model" (CSM) [1], [9]. The CSM is a physically long channel model that takes care of the changing nature of the current. Unfortunately, such a model is not suited for circuit design. An interesting offspring exists, however. It is known as the EKV [3] or ACM [2] model. Because this offspring is a continuous model like the CSM, it

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offers the possibility to calculate derivatives. In other words, it offers the possibility to express g_m/I_D in terms of analytical expressions, which is of great value. We therefore briefly introduce the basic expressions underlying the EKV/ACM model. The singularity of the model is that, when the transistor is saturated, the parameter controlling the drain current is not the gate voltage but the mobile charge density at the source. More precisely, the driving parameter of the model is the normalized mobile charge density q. Another interesting feature resulting from the physics of MOS transistors is that the diffusion current varies like q, whereas the drift current varies like q^2. In short, the drain current of the EKV/ACM model is given by the expression below, which implies the predominance of diffusion or drift current depending on q being either $\ll 1$ or $\gg 1$:

$$I_D = I_S(q^2 + q) \tag{1.8}$$

The factor I_S, the so-called specific current, is defined by expression (1.9) below, where U_T represents the thermal voltage kT/q^e (with k the Boltzmann constant, T the absolute temperature, and q^e the charge of the electron), n the subthreshold slope factor, μ the mobility, C_{ox} the gate-oxide capacitance per micron, and W/L the aspect ratio of the transistor:

$$I_S = 2nU_T\mu C_{ox}\frac{W}{L} = I_{S_{square}}\frac{W}{L} \tag{1.9}$$

A second expression is required in order to finalize the basic EKV/ACM model. It connects the gate voltage V_{GS} to q after the introduction of the threshold voltage V_T:

$$V_{GS} - V_T = nU_T(2(q-1) + \log(q)) \tag{1.10}$$

With the equations above, we can reconstruct drain currents that match nicely any I_D (V_{GS}) characteristics once n, V_T and I_S are identified. Consider for instance the drain current characteristic in the upper part of Figure 1.7, which is taken up by the continuous curve of Figure 1.8. We extract the EKV parameters ($n = 1.2671$, $V_T = 0.4972$ V and $I_S = 4.5718$ μA) from the latter, thanks to the identification algorithm described further, and insert these in (1.7) and (1.10). The

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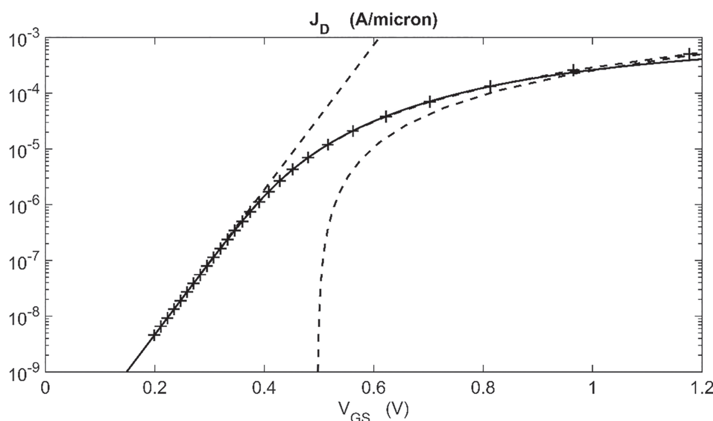

Figure 1.8: The drain current I_D versus the gate-to-source voltage V_{GS} (plain lines) compared to the EKV best fit (+). The other lines represent the exponential and quadratic approximations.

drain current characteristic that we obtain is represented by means of "+" signs in Figure 1.8. The two curves overlap fairly well, except with regard to strong inversion, where the model fails since the basic EKV model ignores velocity saturation.

One of the noteworthy aspects of the above equations is that they bring about well-known approximate expressions for I_D in strong and weak inversion. When $q \gg 1$, eliminating q between (1.8) and (1.10) leads to the strong inversion quadratic equation below, that is illustrated by the dotted curve in the right part of Figure 1.8:

$$I_D = \mu C_{ox} \frac{W}{L} \left(\frac{V_{GS} - V_T}{2} \right)^2 \tag{1.11}$$

Similarly, in weak inversion, when $q \ll 1$, the same thought ends up with the exponential expression below, represented by the dashed straight-line tangent to the I_D (V_{GS}) characteristic at low V_{GS}:

$$I_D = I_{Do} \exp \left(\frac{V_{GS}}{nU_T} \right) \tag{1.12}$$

The factor n appending the thermal voltage in the above expression implies that, the growth rate of I_D in weak inversion is a little slower than with bipolar transistors, where n is equal to one indeed. Bulk

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MOS transistors show values of n that are generally comprised between 1.2 and 1.5, depending on the substrate doping, which is due to the existence of the back-gate.

Moreover, what Figure 1.8 shows clearly is that a large open space exists in the middle where none of the two approximate expressions above, (1.11) and (1.12), apply. In this region, the so-called "moderate inversion" region, the values of q range from 0.1 to 10. The point is that most CMOS circuits nowadays operate in this region as moderate inversion combines good speed and power consumption.

Since the EKV model is a continuous model, we can figure out an analytic expression for the transconductance efficiency. To this end, we take the middle expression of (1.6), compute the derivative with respect to q of the drain current I_D given by (1.8), divide the result by the derivative with respect to q of (1.10), and, finally, divide the outcome by I_D. What we obtain is the expression below illustrated by means of "+" signs in Figure 1.9:

$$\frac{g_m}{I_D} = \frac{1}{nU_T}\frac{1}{q+1} \tag{1.13}$$

The graphical representation of the latter coincides remarkably well with the original curve, except, as expected, in strong inversion owing to lack of velocity saturation modeling. In weak inversion, according

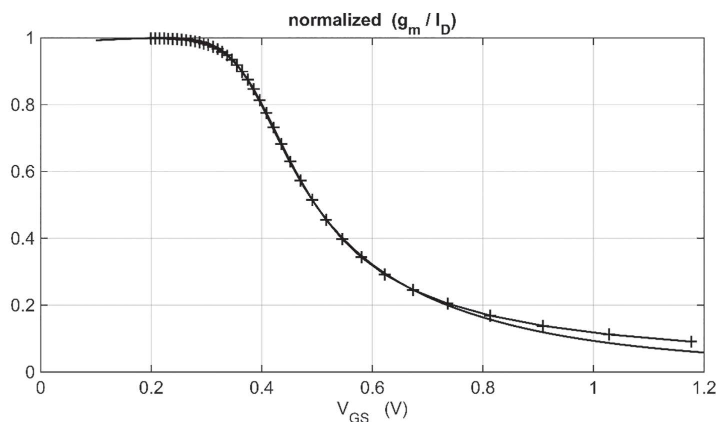

Figure 1.9: The normalized transconductance efficiency of the EKV/ACM model (1.13) represented by "+" is compared to the result obtained in Figure 1.7.

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to (1.13), the transconductance efficiency comes down to $1/(nU_T)$, with magnitudes generally lying between 20 and 30 S/A. As q rises, the transconductance efficiency decays swiftly through moderate inversion and then more slowly in strong inversion. When $q \gg 1$, (1.13) turns into $1/(nU_T \cdot q)$, which boils down to the expression below using (1.10):

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_T} \tag{1.14}$$

Making q equal to one defines a point at mid-height of the g_m/I_D curve of Figure 1.7, where, according to (1.10), the gate-to-source voltage is equal to V_T while the drain current equals twice I_S according to (1.8). Since we can extract the subthreshold factor n from the maximum of g_m/I_D in weak inversion, expression (1.13) paves the way towards the acquisition of the EKV parameters.

Another interesting thought we learn from expressions (1.13) is that once g_m/I_D is fixed, we know q, hence we know the gate voltage V_{GS} through (1.10). Although the connection between the transconductance efficiency and the gate-to source voltage is not as obvious as the EKV expressions show, there is an important message here. We frequently take V_{GS} as a driving parameter, but we could take g_m/I_D as well. By this, we get a better control of the mode of operation of the transistor, whether it is strong, weak or moderate inversion. When we consider V_{GS}, we work blindly, as we don't know in which operating mode the transistor is truly operating. V_{GS} is affected indeed by any threshold voltage modifications caused by back-bias or gate length modifications, not mentioning interface states, all items that the transconductance efficiency ignores almost. In other words, instead of controlling the drain current density and the low-frequency gain through V_{GS}, like we did in Figure 1.6, we can call out g_m/I_D using the expressions below, which leads us to Figure 1.10:

$$\text{JD} = \text{lookup}\,(\text{nch}, \textbf{`ID_W'}, \textbf{`GM_ID'}, \text{gm_ID}, \textbf{`L'}, \text{L}); \tag{1.15}$$

$$\text{Avo} = \text{lookup}\,(\text{nch}, \textbf{`GM_GDS'}, \textbf{`GM_ID'}, \text{gm_ID}, \textbf{`L'}, \text{L}); \tag{1.16}$$

One may argue that taking g_m/I_D as driving parameter may not be a good idea deep in weak inversion as the magnitude of the transconductance efficiency tends to become constant in this mode of operation. We

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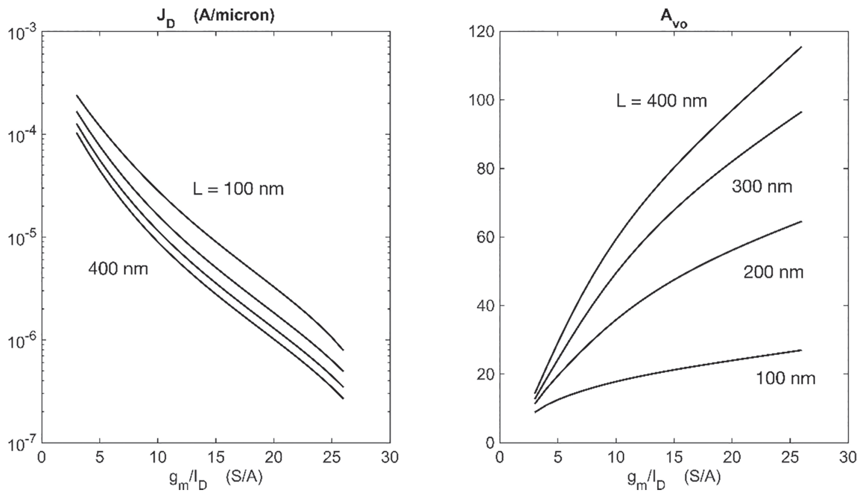

Figure 1.10: Drain current density and open-drain low-frequency gain of the common-source stage versus g_m/I_D for four different gate lengths.

can get around this difficulty by substituting **'ID_W'** for **'GM_ID'** since deep in weak inversion, the drain current density varies like q. To assess data in this mode of operation, we replace **GM_ID** by **ID_W** in (1.15) and (1.16).

Turning g_m/I_D or I_D/W into a driving parameter doesn't dismiss V_{GS} of course. Like in expression (1.10), which relates V_{GS} to q, we introduce the two additional Lookup Functions listed under (1.17) to ascertain V_{GS} knowing g_m/I_D or J_D:

$$V_{GS} = \text{lookupVGS}(\text{nch}, \textbf{'GM_ID'} \text{ or } \textbf{'ID_W'}, \ldots, \textbf{'VDS'}, \ldots, \textbf{'VSB'}, \ldots, \textbf{'L'}, \ldots)$$

or

$$V_{GS} = \text{lookupVGS}(\text{nch}, \textbf{'GM_ID'} \text{ or } \textbf{'ID_W'}, \ldots, \textbf{'VDB'}, \ldots, \textbf{'VGB'}, \ldots, \textbf{'L'}, \ldots) \tag{1.17}$$

The Transit Frequency f_T

The transit frequency f_T (**'GM_CGG'**) is another important class-2 parameter. It defines the frequency that makes the *current* gain A_i of the common-source transistor with shorted output equal to unity. At

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a first glance, the current gain is not a very appealing concept. We usually do not care about gate input currents for these are supposed to be negligible. The input capacitance C_{gg}, which totalizes C_{gs}, C_{gb} and C_{gd}, indeed draws little current in comparison to the current delivered by the controlled output current source of the transistor. Nonetheless, as the frequency increases, the gate input current steadily grows while the output current of the shorted output common-source stage remains unchanged. Hence, the current gain decreases gradually until we reach the so-called transit frequency f_T equal to $g_m/2\pi C_{gg}$, where the input and output currents become equal.

The reason that the transit frequency concept is important is because f_T is a marker that warns us about the legitimacy of the QSM model. A conservative rule of thumb consists in making the assumption that, apart from weak inversion, the QSM model ceases to represent the behavior of MOS transistors faithfully as soon as the frequency surpasses f_T divided by a factor say 4 or 10. Above this frequency, the transistor is still usable, but simulations using SPICE models risk to induce improper conclusions. Hereafter, we take the view of never exceeding $f_T/10$. This does not really restrain the design space in practice as we know that short-channel devices commonly achieve f_T values in excess of 100 GHz. The transit frequencies that are achieved with the technology adopted in this work are shown in Figure 1.11, as a function of V_{GS} in the left figure and as a function of g_m/I_D in the right figure. The graphs were generated from the two expressions below:

$$f_T = \text{lookup}(\text{nch}, \textbf{`GM_CGG'}, \textbf{`L'}, \text{L})/(2 * \text{pi});$$

and

$$f_T = \text{lookup}\,(\text{nch}, \textbf{`GM_CGG'}, \textbf{`GM_ID'}, \text{gm_ID}, \textbf{`L'}, \text{L})/(2 * \text{pi}); \tag{1.18}$$

1.3 Sizing and Optimization Through the use of Lookup Tables

We now review an example that illustrates the possibility to combine sizing and optimization via Lookup Tables. We consider the common-source transistor M_1 of Figure 1.12. The device is fed by an ideal current

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source I_D and loaded by a capacitor C_L equal to 1 pF. The output voltage V_{out} is fixed at 0.6 V by means of a low-pass feedback loop that controls the gate voltage V_{in}. We search the drain current I_D, the gate

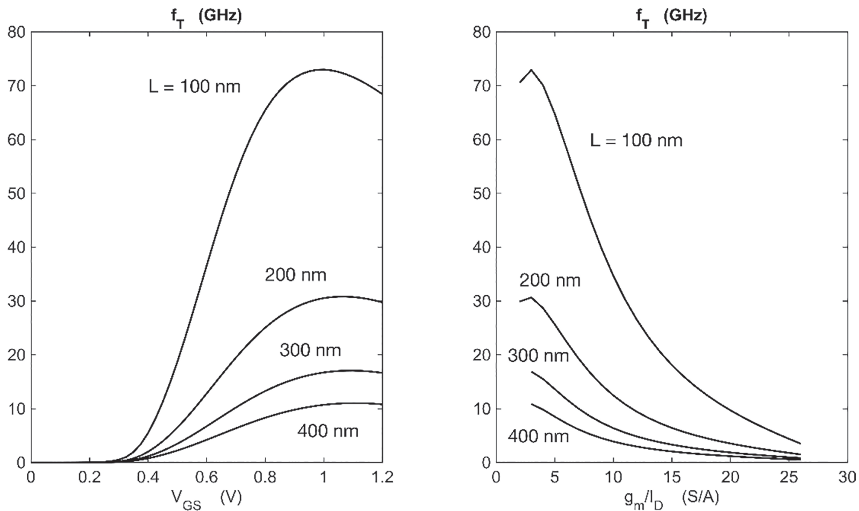

Figure 1.11: The transit frequency f_T as a function of V_{GS} (left) and g_m/I_D (right) for different gate lengths.

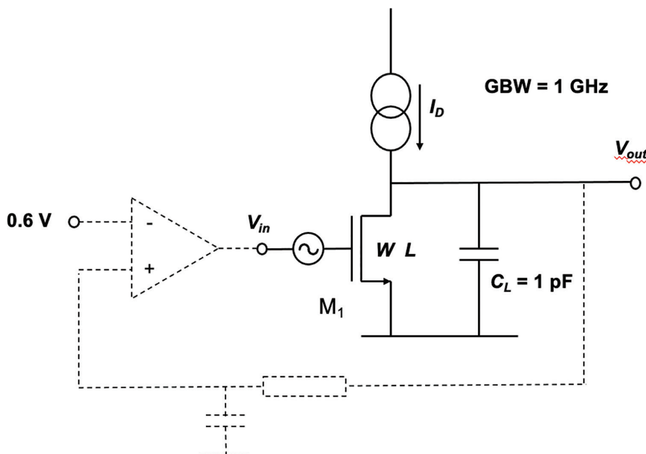

Figure 1.12: Design example: find I_D, W and L that maximize A_{vo} with f_u = 1 GHz.

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width W and the length L that maximize the low-frequency gain while achieving a unity-gain frequency f_u (or gain-bandwidth product GBW) of 1 GHz.

We replace M_1 by its QSM equivalent circuit, omitting the parasitic capacitances since the load capacitor C_L outweighs these. Because the circuit now comes down to a first-order system, its frequency response contains a constant-gain segment followed by a section where the gain decays continuously at the rate of -20 dB/decade. Since the unity-gain frequency f_u is equal to $g_m/2\pi C_L$, the transconductance g_m of M_1 is fixed at:

$$g_m = 2\pi f_u C_L = 6{,}283\ 10^{-3}\ \mathrm{S} \tag{1.19}$$

The problem consequently boils down to the search of values for I_D, W and L that maximize the low-frequency gain A_{vo} while satisfying (1.19). Moreover, in order to warrant the legitimacy of the QSM model, the transit frequency f_T should equal (or exceed) ten times f_u, thus 10 GHz. The way we proceed is illustrated in Figure 1.13, which displays two sets of curves considering four gate lengths varying from 0.1 to 0.4 μm. On the left in the figure, we see the transit frequency f_T versus g_m/I_D reported in Figure 1.11 and, on the right in the same figure, the low-frequency gain A_{vo} versus g_m/I_D of Figure 1.10, both sharing the same vertical axis. We draw the horizontal dotted line at 10 GHz representing the lower boundary of f_T and mark with asterisks the crossings with the curves representing the achievable transit frequencies versus the gate length. These crossings define the transconductance efficiencies (marked by dotted vertical lines) wherefrom we assess the gains (marked by small circles). To conclude, we construct the broken-line curve called the constant-f_T gain locus that enables us to see how the gain changes as we modify the gate length. From inspection, the largest gain we can reach is 40, for L being equal to 0.2 μm and (g_m/I_D) 12 S/A. This is the best we can do. If we had chosen a larger f_T, the dotted horizontal line would have shifted upwards, automatically limiting the range of possible (g_m/I_D) values, thereby reducing also the gain. For instance, if we make f_T equal to 20 GHz, the maximal gain we can get is 27, g_m/I_D being equal to 8.2 S/A, and L 0.175 μm. Making f_T larger than the recommended 10 times f_u does not bring any benefit, on the

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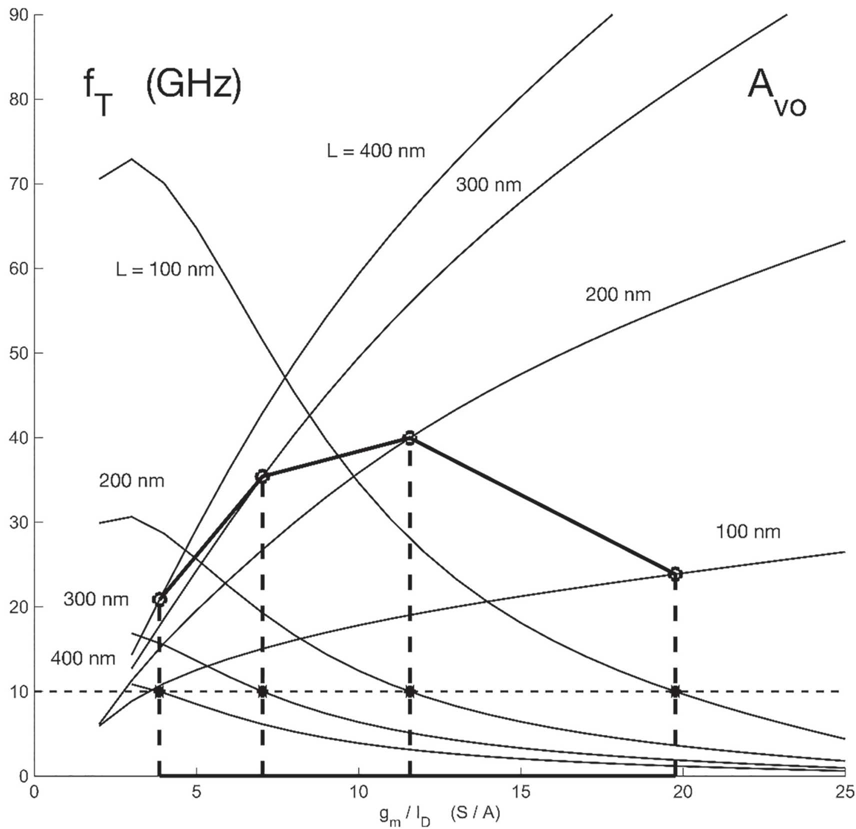

Figure 1.13: The search for L and g_m/I_D values maximizing A_{vo}, while meeting a GBW of 1 GHz.

contrary! We now translate this sizing procedure in terms of Matlab instructions:

$$g_m_I_D = \text{lookup}(\text{nch}, \textbf{`GM_ID'}, \textbf{`GM_CGG'}, 2 * \text{pi} * f_T, \textbf{`L'}, \text{L}) \tag{1.20}$$

$$A_{vo} = \text{diag}(\text{lookup}(\text{nch}, \textbf{`GM_GDS'}, \textbf{`GM_ID'}, g_m_I_D, \textbf{`L'}, L)) \tag{1.21}$$

The first line shapes the g_m/I_D vector meeting the desired transit frequency considering an extended range of gate lengths L. The second line derives the low-frequency gain vector A_{vo} from the g_m/I_D vector

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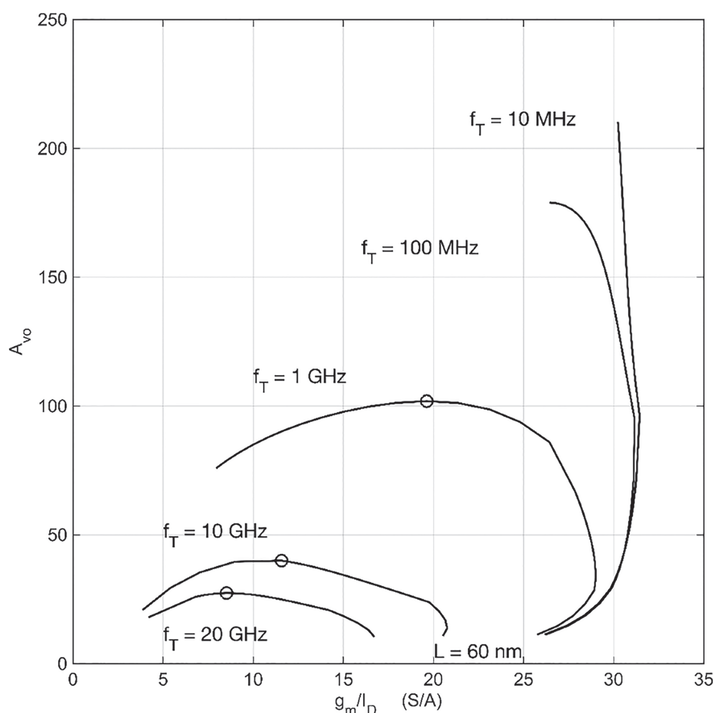

Figure 1.14: Constant-f_T loci of the low-frequency gain A_{vo} as a function of the transconductance efficiency for transit frequency f_T values ranging from 20 GHz down to 10 MHz.

we just got considering the same gate lengths vector L. The outcome is shown in Figure 1.14 for different transit frequency values. The 10-GHz constant-f_T locus of Figure 1.14 reproduces the locus we already got in Figure 1.13 but with a denser gate lengths vector. When L is small (60 to 100 nm), the transistor operates in moderate near weak inversion. The gain does not exceed 20, while g_m/I_D does not change much remaining near 20 S/A. As L increases, the gain grows until it reaches the maximum (value of 40) marked by a circle, g_m/I_D and L being equal to 11.58 S/A and 0.20 μm, respectively. Beyond this, the gain decreases continuously while the transistor progressively enters in strong inversion.

So far, I_D and W are still unknown! To assess the drain currents that meet the desired f_T, all we need to do is to divide the constant

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transconductance g_m of (1.19) by g_m/I_D and, for what concerns the gate width W, divide the drain currents by the subsequent drain current densities:

$$I_D = g_m/(g_m/I_D) \tag{1.22}$$

$$J_D = \text{lookup}(\text{nch}, \textbf{`ID_W'}, \textbf{`GM_ID'}, g_m/I_D, \textbf{`L'}, L) \tag{1.23}$$

If our objective is to get the largest gain, the drain current we must choose is equal to 543 μA and the gate width 49.6 μm. If power consumption is a concern and we are ready to sacrifice a little gain, we can increase g_m/I_D by lowering W. For instance, if we increase g_m/I_D by 10%, the power consumption reduces with the same amount, while the gain loss is only 3.6%.

We did not consider the gate-to-source voltage so far. We didn't need V_{GS} in any event, but we can still assess its magnitude using (1.17), finding that V_{in} is equal to 0.5847 V when the gain is the largest.

To verify the above results, we have run a SPICE simulation of the circuit of Figure 1.12 and obtained a low-frequency gain of 40.0 with a gain-bandwidth product of 0.937 GHz. This 3.3% bandwidth difference is presumably due to the fact that – different from the simulator – we did not take the parasitic capacitances into consideration.

In Figure 1.14, we consider a few more transit frequencies than the original 1 GHz. As f_T lessens, the maximum gain we can achieve (marked by circles) and the transconductance efficiency increase. If we make f_T equal to 1 GHz, the maximum achievable gain rises to 102, while the transconductance efficiency reaches 19.63 S/A. The unity-gain frequency f_u being equal to 100 MHz ($f_T/10$), the drain current I_D drops to 32 μA, while the gate length and width become 0.45 and 32.40 μm, respectively. Lowering the transition frequency further drives the constant-f_T loci further into weak inversion. Ultimately, the constant-f_T loci become vertical lines, as the drain current tends to become constant whatever unity-gain frequency we choose. The parameter that controls the gain is now the drain current density.

What can we conclude from this design example? We were able to assess currents and transistor sizes in order to reach prescribed performance objectives. The parameters we extracted from the Lookup Tables granted realistic values that enabled us to derive circuits with

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performances that agreed nicely with the verification simulations. Not only did we avoid re-iterated simulations, but we also sensed the way how we could change the design parameters in order to extend our search. In the second part of this monograph, we apply the ideas and design methodology developed in the first part towards two practical design examples.

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